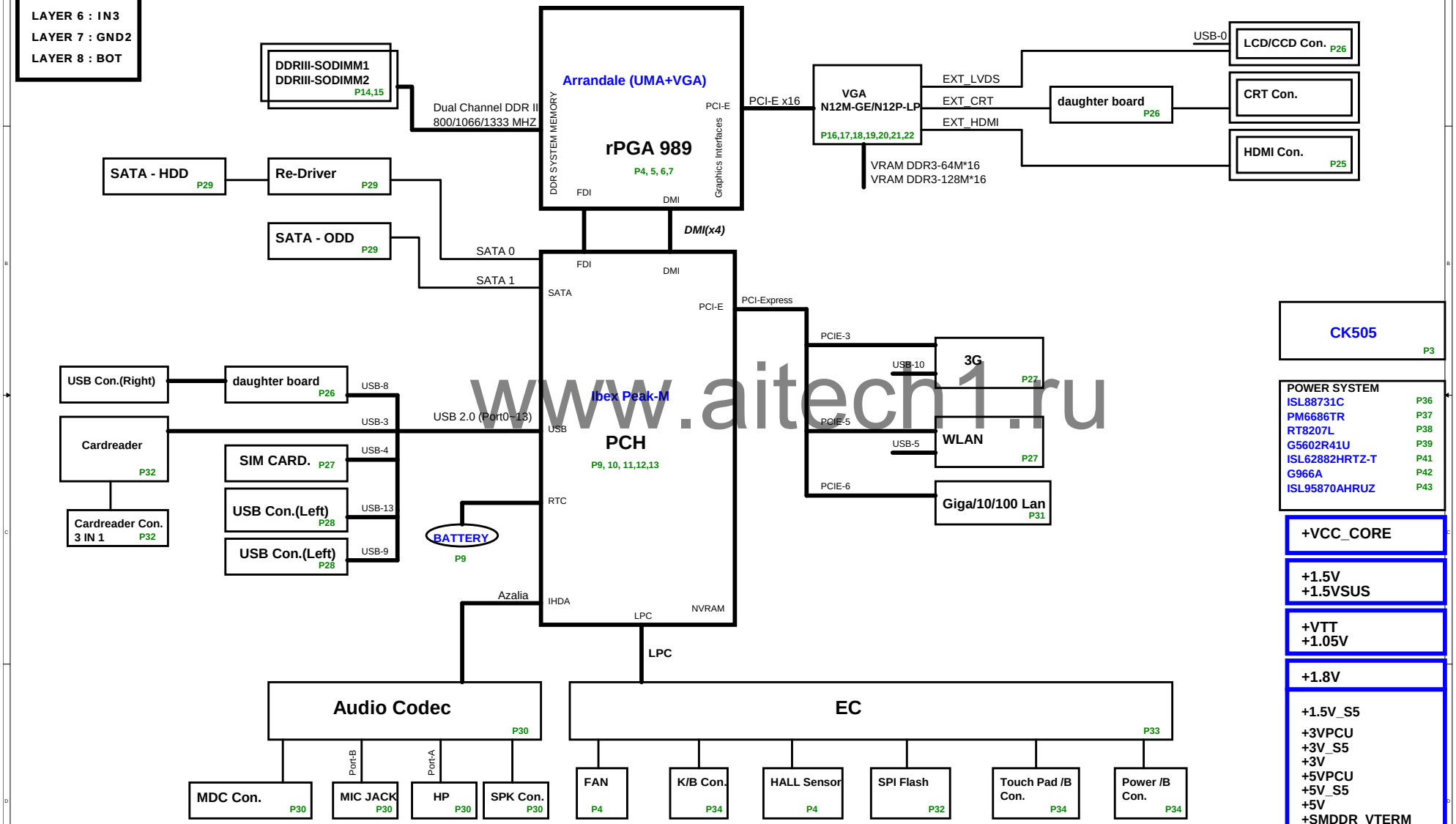
TE4D Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT



CK505 P3

POWER SYSTEM

ISL88731C	P36
PM6686TR	P37
RT8207L	P38
G5602R41U	P39
ISL62882HRTZ-T	P41
G966A	P42
ISL95870AHRUZ	P43

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5

+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	Block Diagram	1A

Date: Friday, November 12, 2010 Sheet 1 of 46

Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

GND PLANE	PAGE
8769AGND	33
Audio_GND	30
Shield_GND	30
GND	ALL
ISL95870A_AGND	30

Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	POWER STAGE AND BOI-FUNCTION	1A

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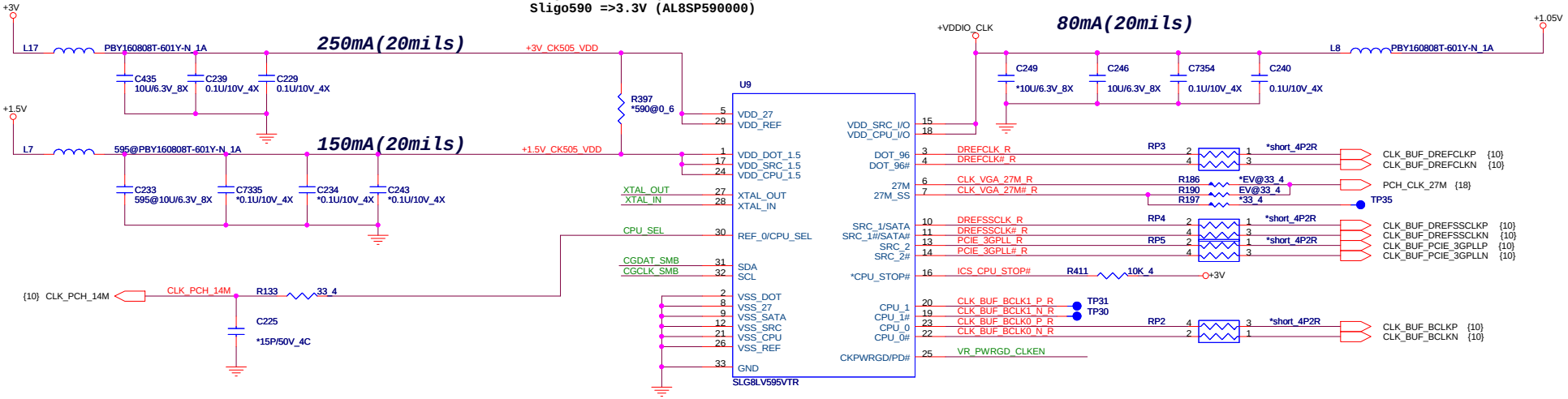
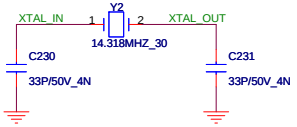
CLOCK Gen [CLK]

03

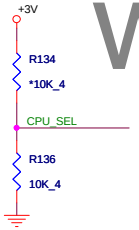
Pin1/17/24
Sligo595 =>1.5V (AL000595000)
Sligo590 =>3.3V (AL8SP590000)



CLK CRYSTAL

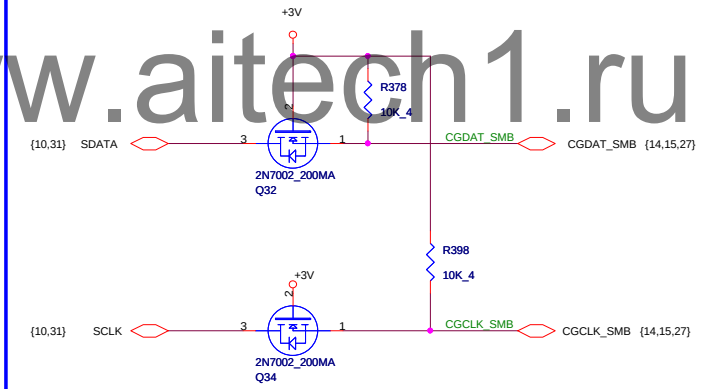


CLK CPU_SEL

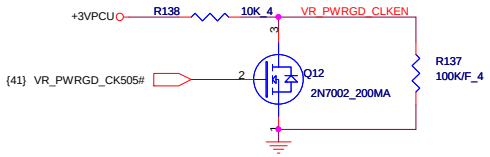


	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



CLK POWERGOOD



Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	CLOCK GENERATOR	A1A
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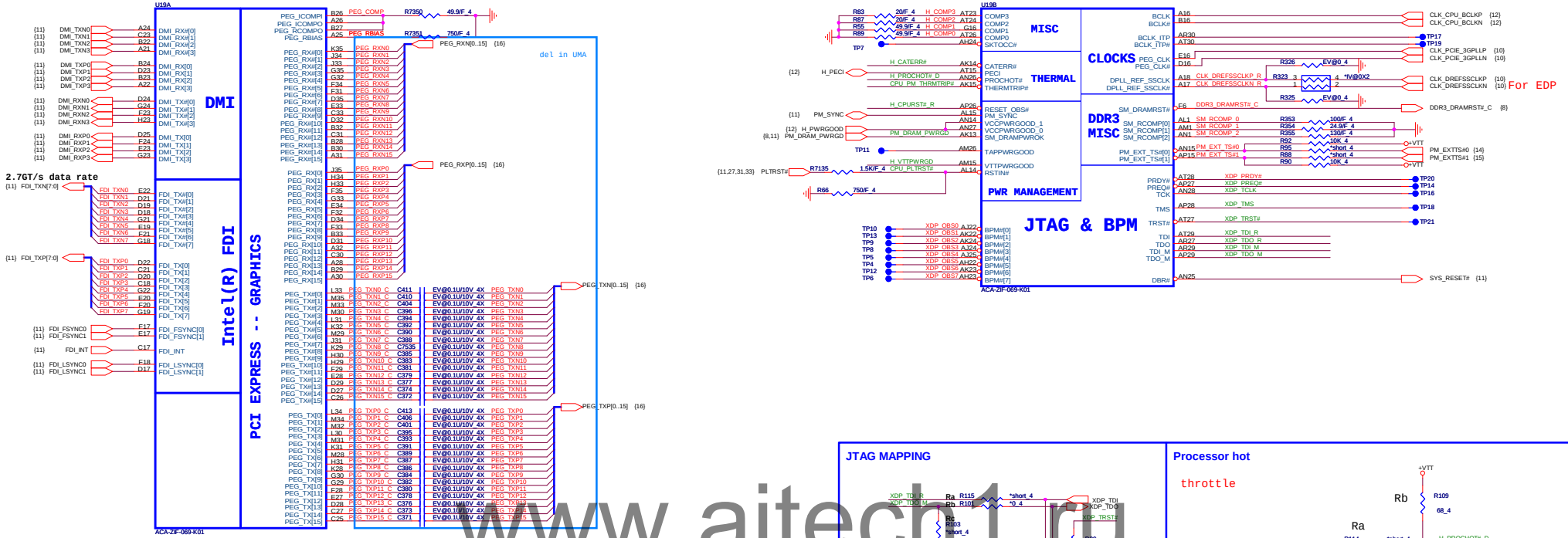

JTAG MAPPING

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

Processor hot

throttle

If Ra no stuff must change Rb to 50 ohm

Thermal Trip

VTT Power Good

Cost Down Study

FDI Disable (Discrete only)

Local Temperature

C3A

#Shut down on 86 degree#

D3B

CPU FAN CTRL

3mA(40mils)

40mils

Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	A1A
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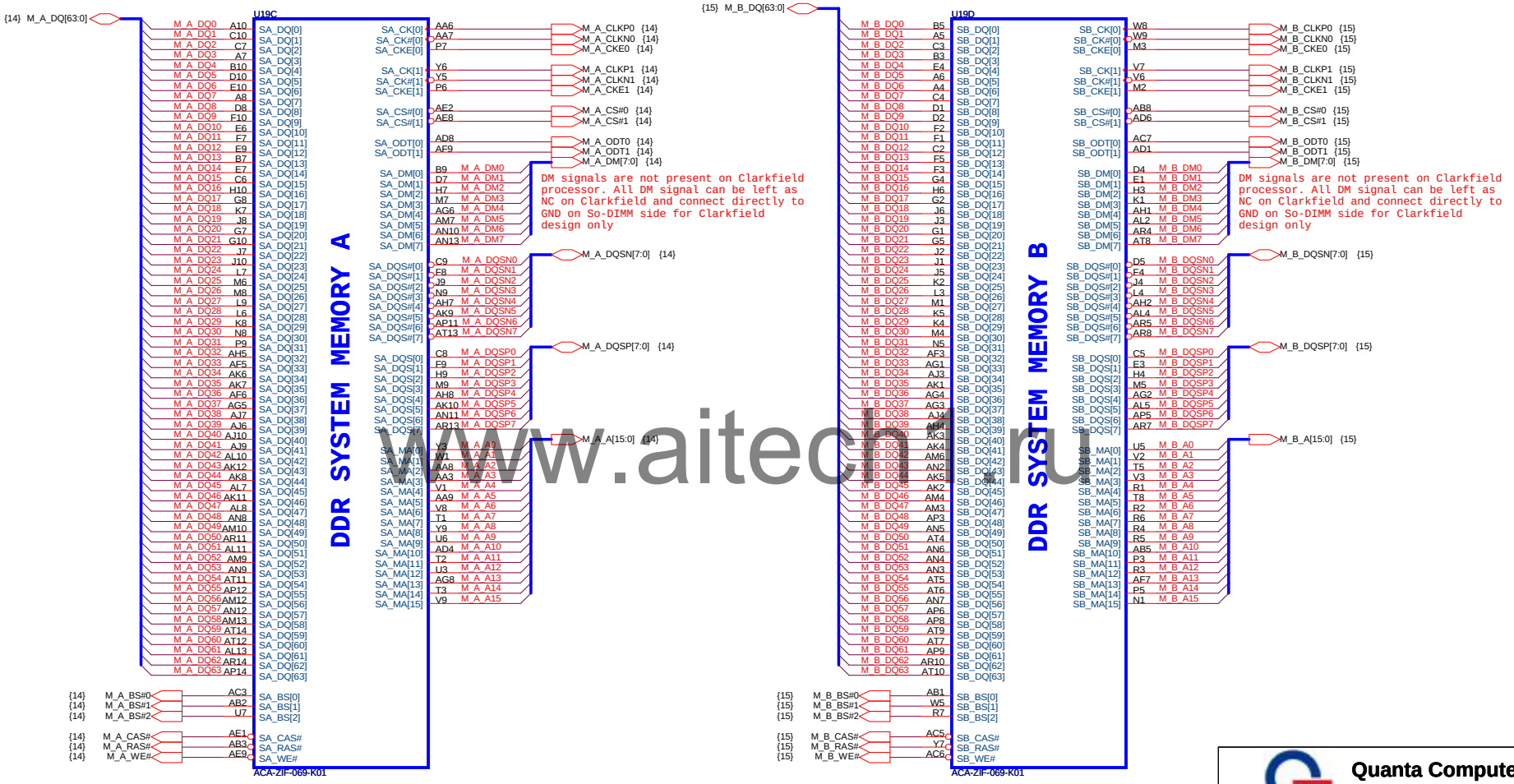
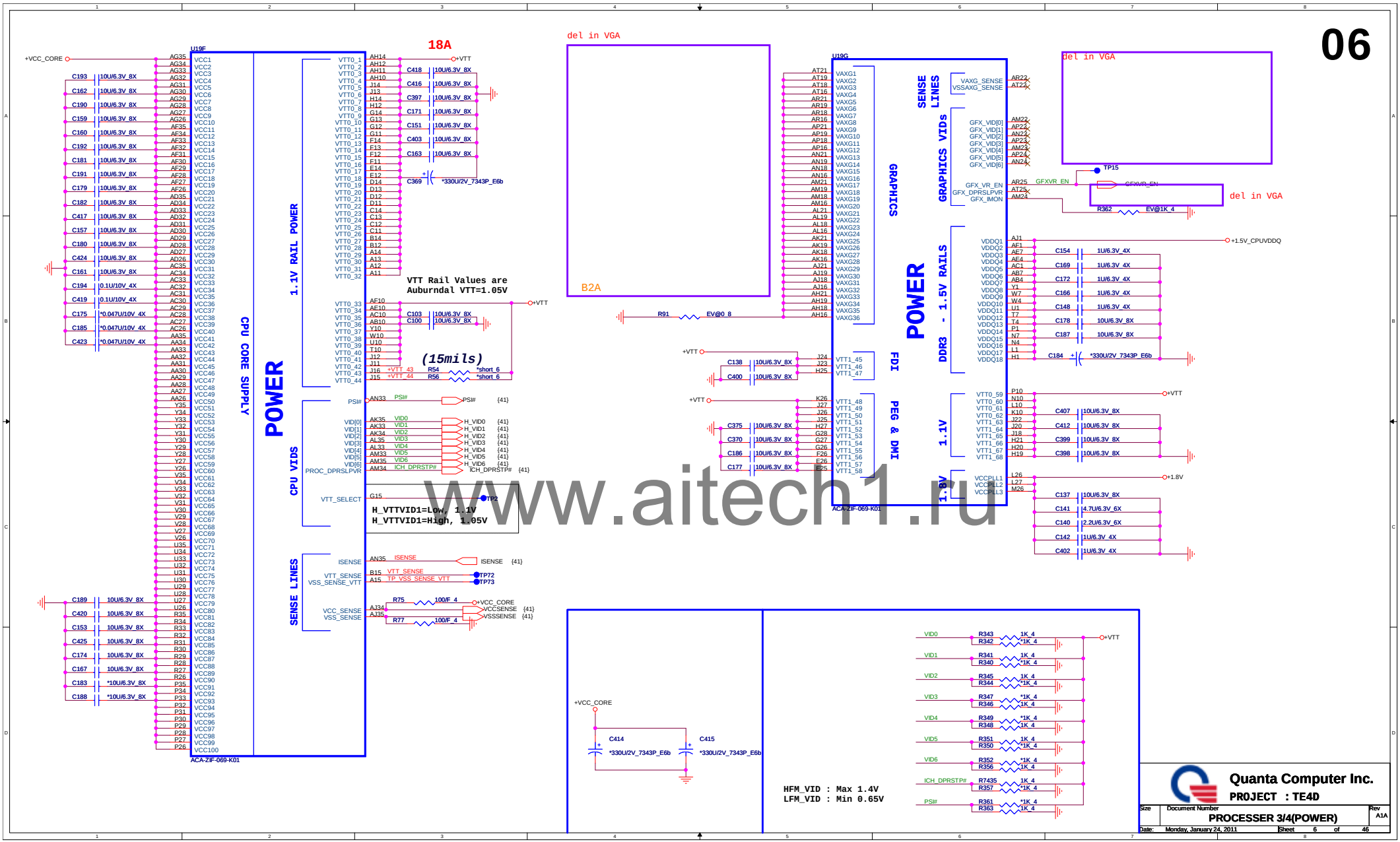
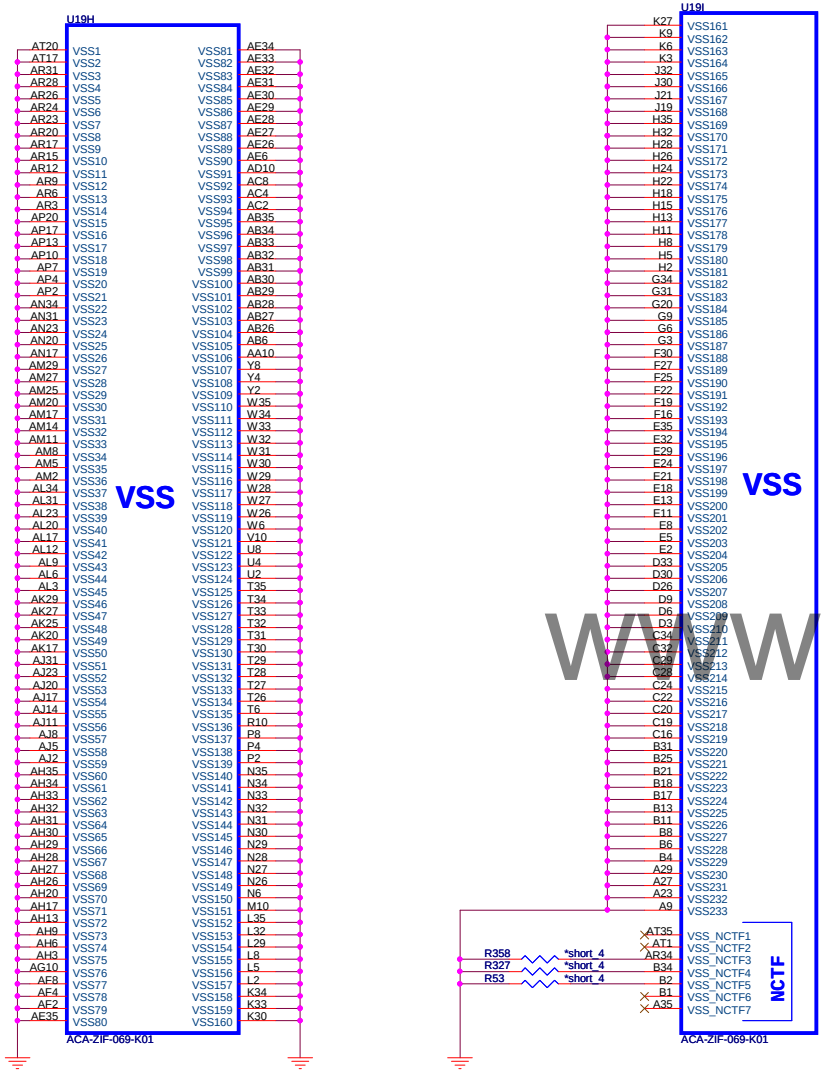
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



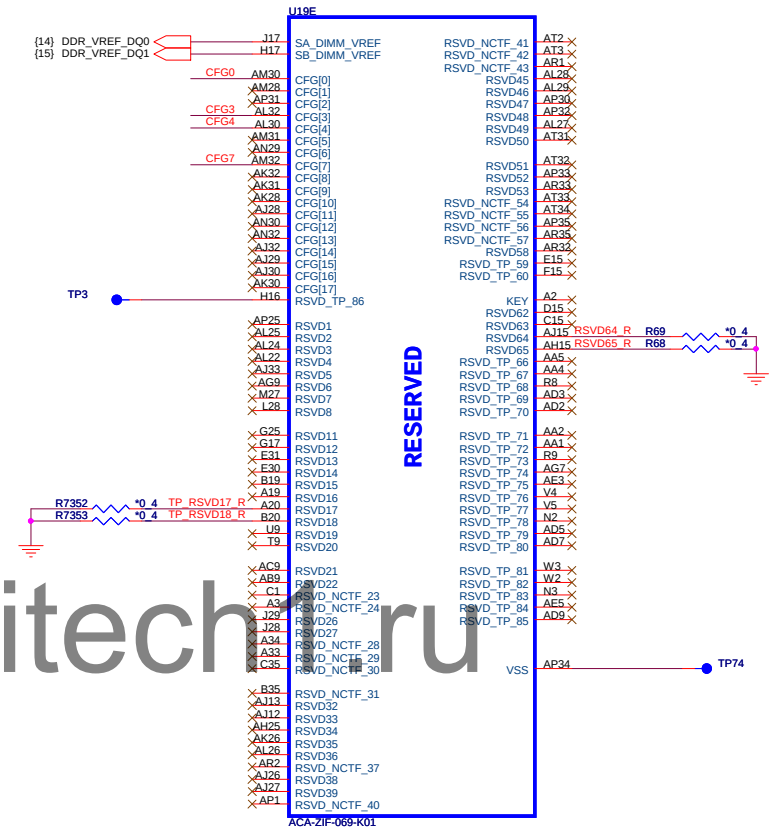
Quanta Computer Inc.		
PROJECT : TE4D		
Size	Document Number	Rev
	PROCESSER 2/4(DDR)	A1A
Date: Monday, January 24, 2011	Sheet 5 of 46	



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



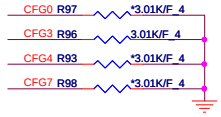
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	A1A

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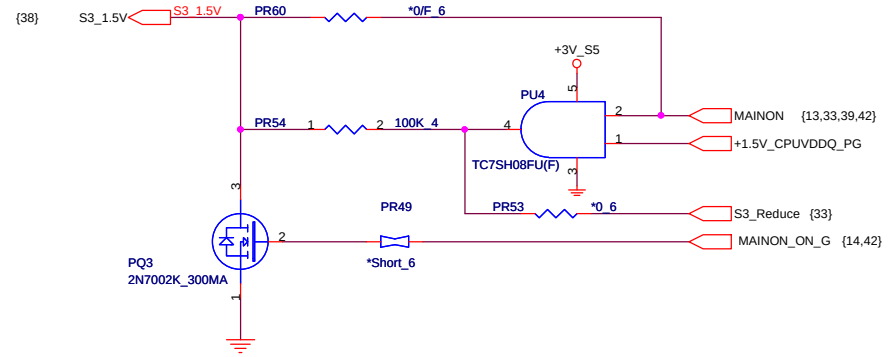
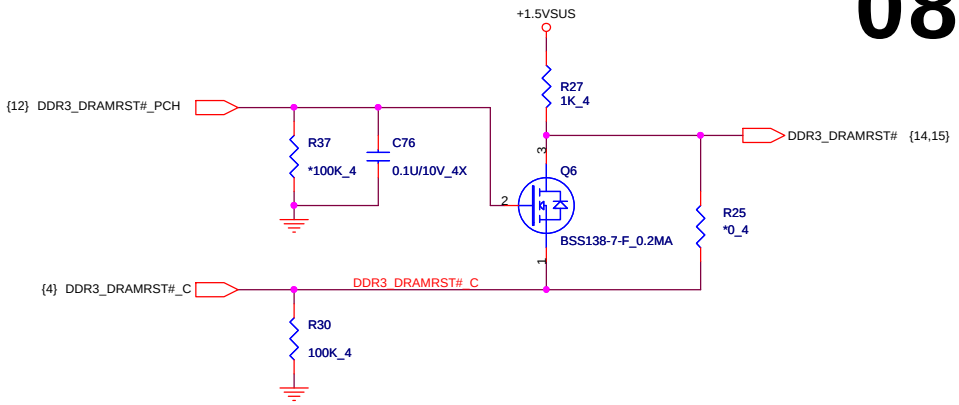
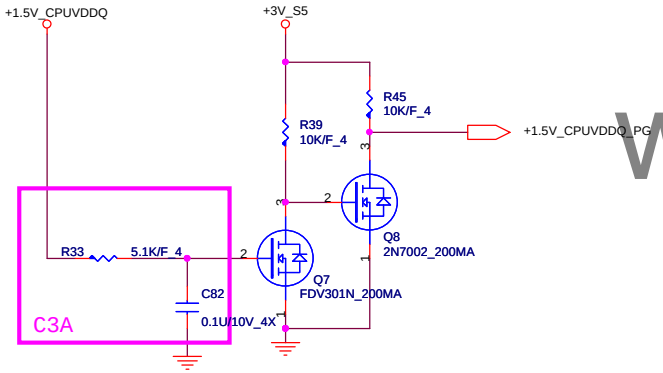
S3 Power Enable



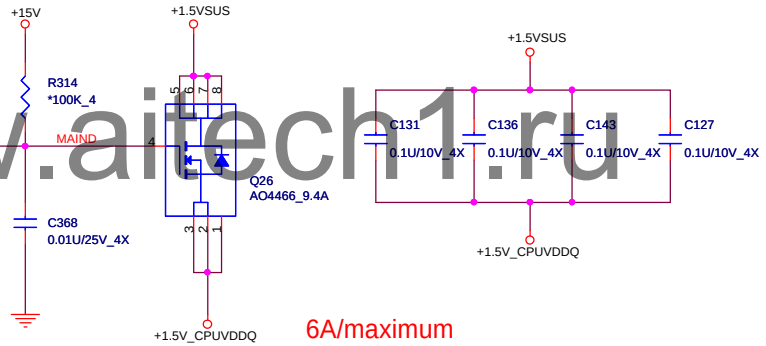
DRAM Reset



VDDQ Power Good



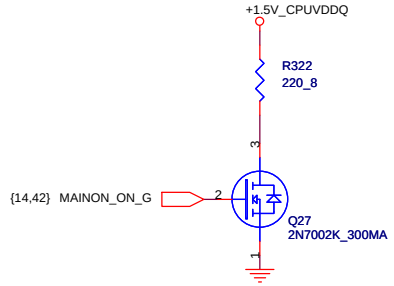
VDDQ Power Switch



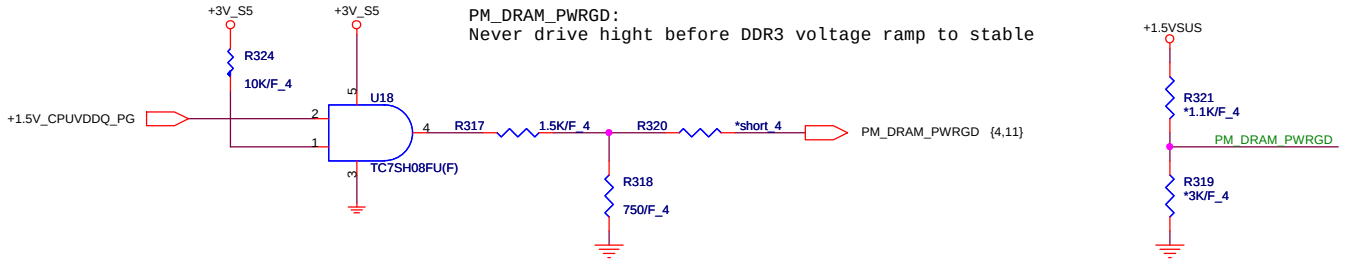
6A/maximum

Q7044可換AO6402A,cost down.

VDDQ Discharge



DRAM Power Good



PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable

Quanta Computer Inc.		
NB7 PROJECT : TE4D		
Size	Document Number: S3 Power Reduction	Rev: A1A
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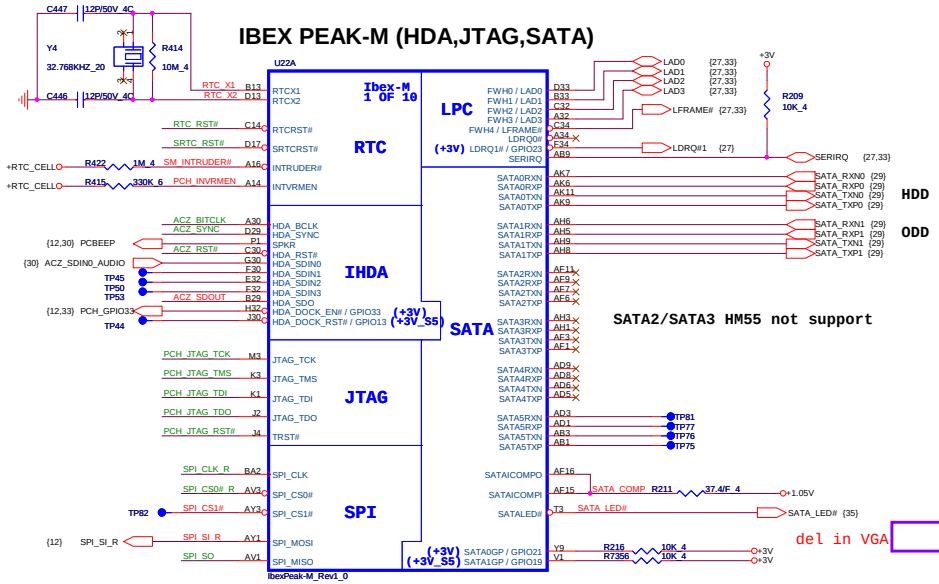
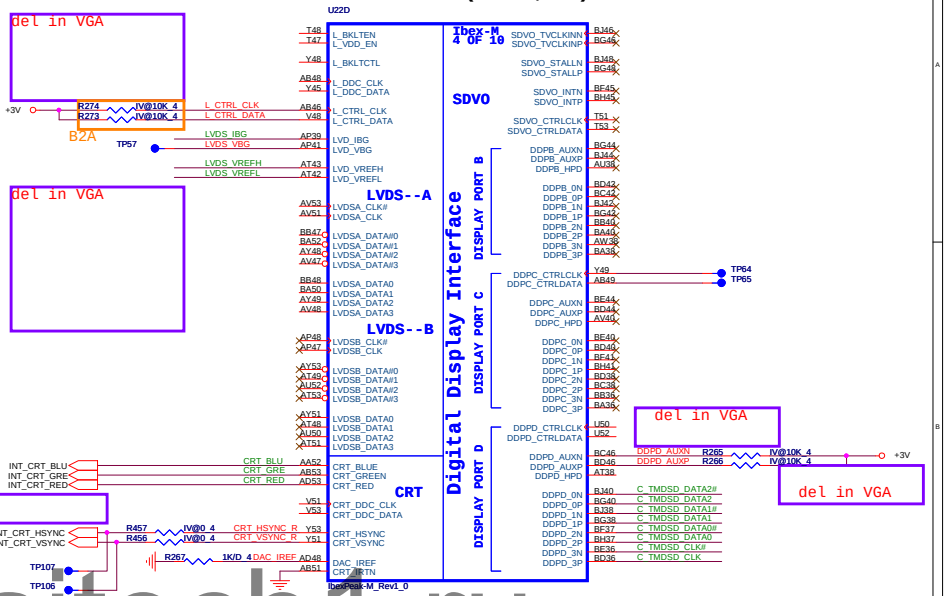
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

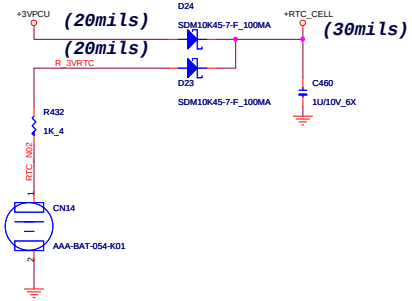


IBEX PEAK-M (LVDS,DDI)



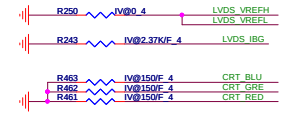
[RTC]

RTC BATTERY

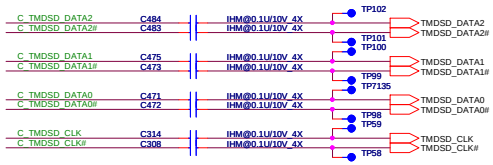


DDP Setting

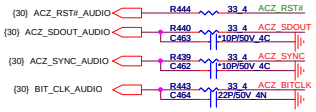
Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

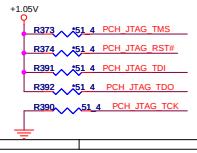


HDMI

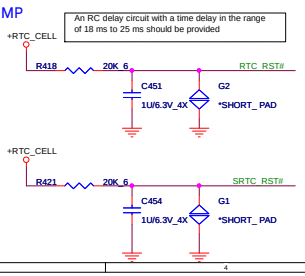


Alzia

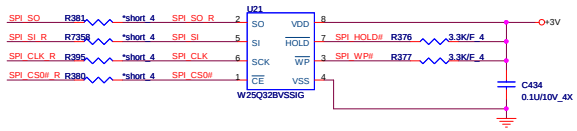




RESET JUMP



4M byte SPI ROM



PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	A1A
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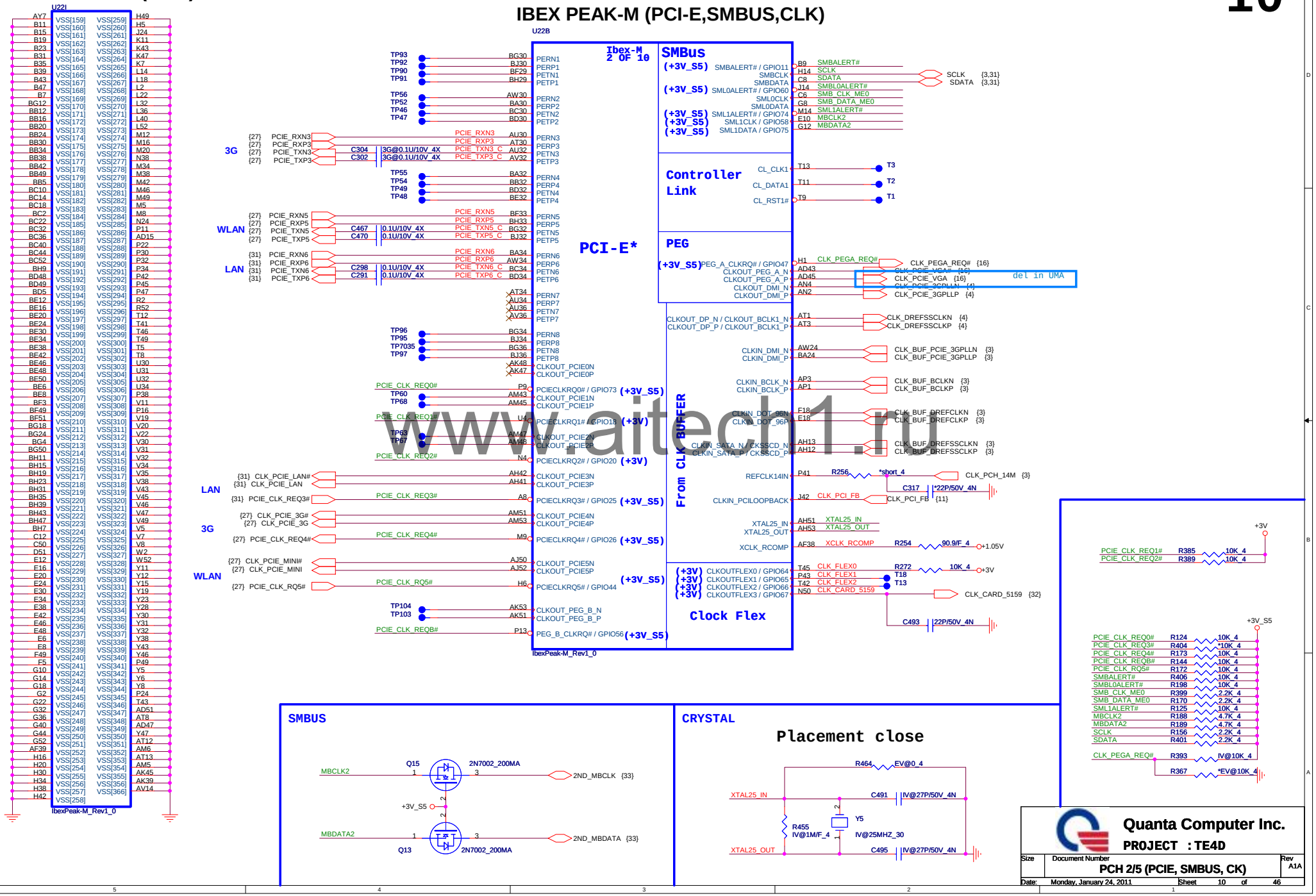
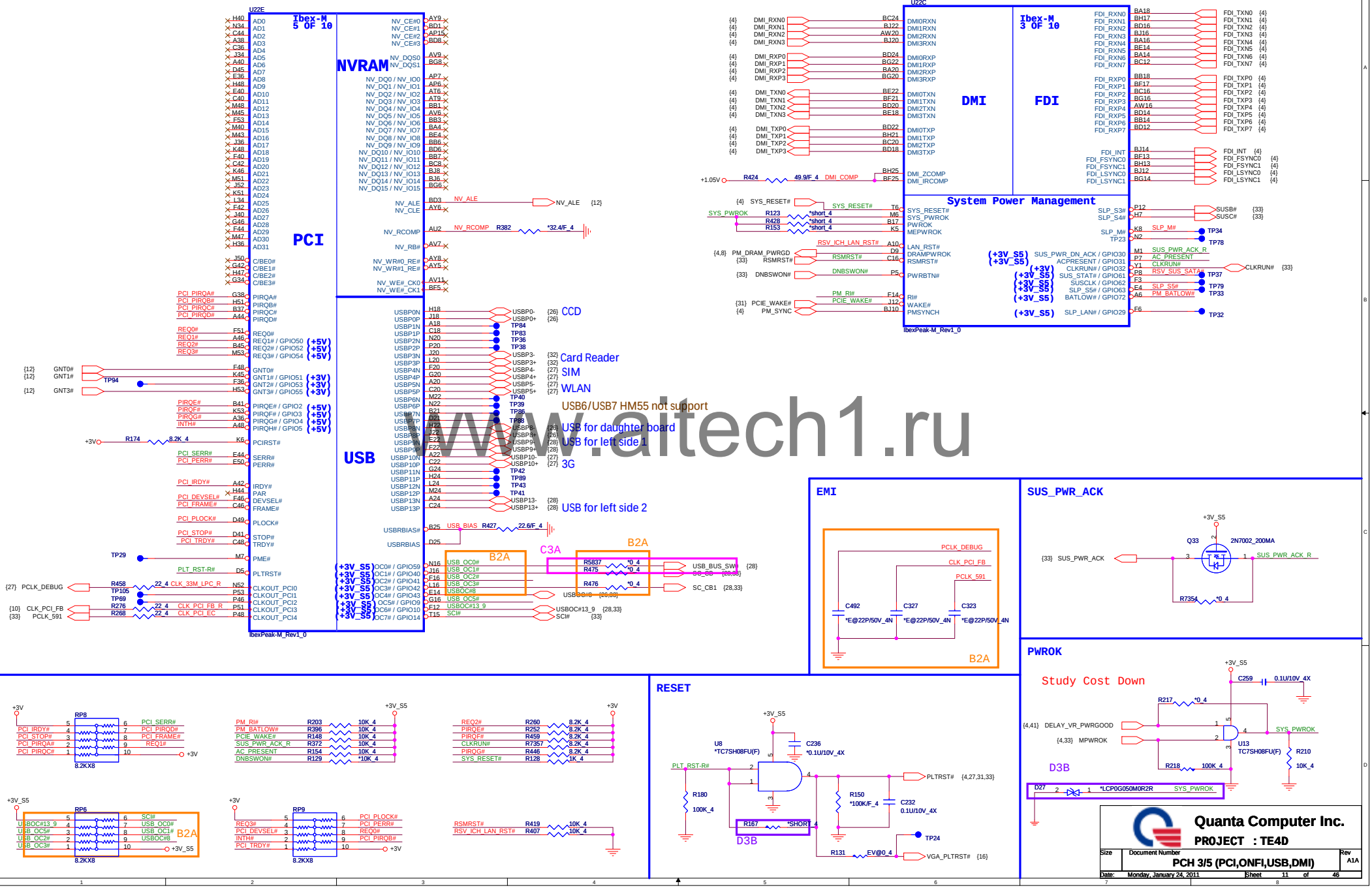
IBEX PEAK-M (GND)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

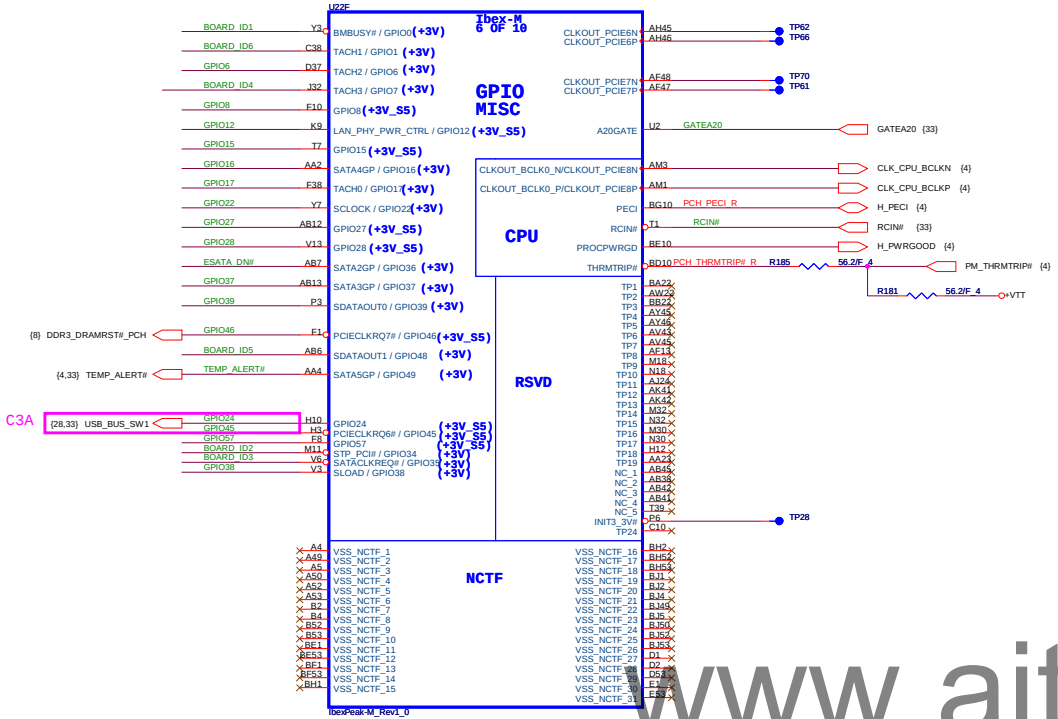


IBEX PEAK-M (PCI,USB,NVRAM)

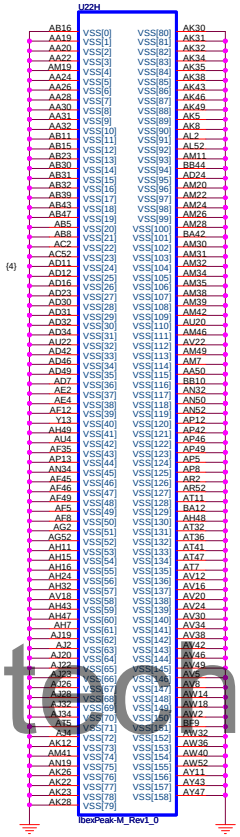
IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

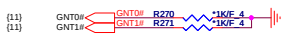
GNT3#/ GPIO55

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #/GPIO33

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#



Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

NV_ALE

1 = Enabled
0 = Disabled (Default)

GPIO8

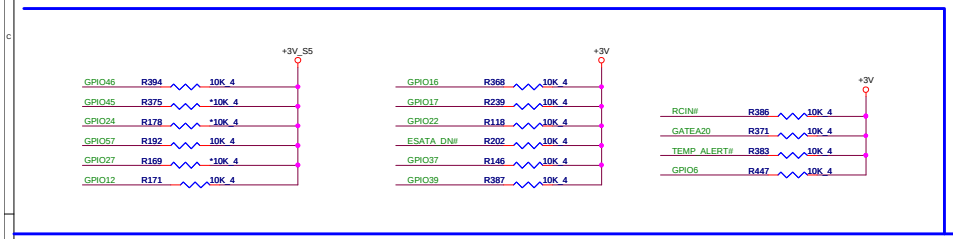
This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

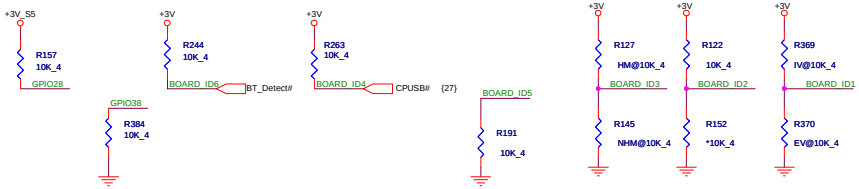
GPIO27

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	GPIO28	GPIO38
UMA SKU VGA SKU	H L							
W/ MDC W/O MDC		H L						
W/ HDMI W/O HDMI			H L					
W/O 3G W/ 3G				H L				
15" 14"					H L			
W/O BT W/ BT						H L		
14 or 15 13							H L	
Old HW(2010) New HW(2011)								H L



Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	A1A
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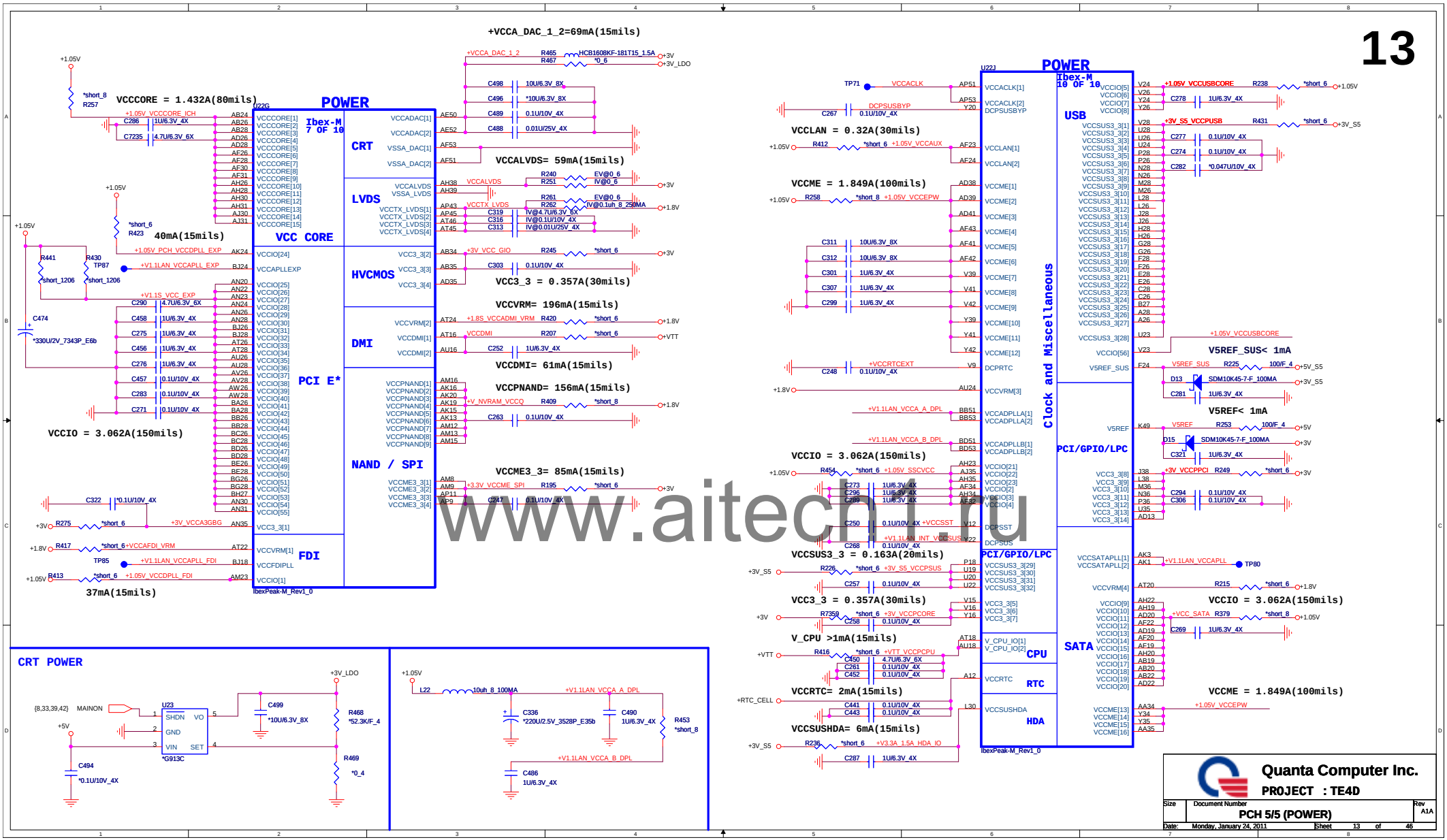

Quanta Computer Inc.

PROJECT : TE4D

Size	Document Number	Rev
	PCH 5/5 (POWER)	A1A
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H=4

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRSK-20401-TP4B

JDIM2B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRSK-20401-TP4B

B2A

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

Quanta Computer Inc.		
PROJECT : TE4D		
Size	Document Number: DDR3 DIMM-0	Rev: A1A
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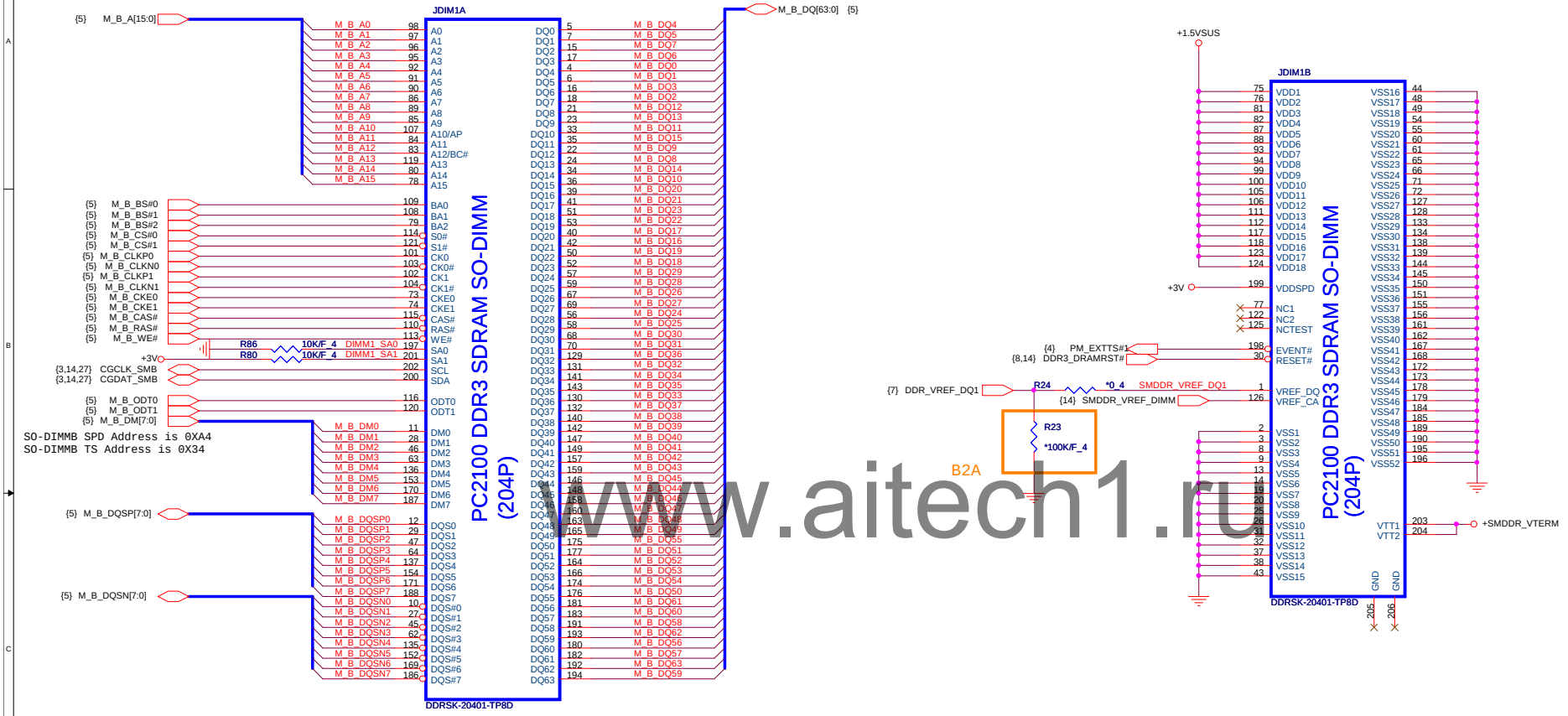
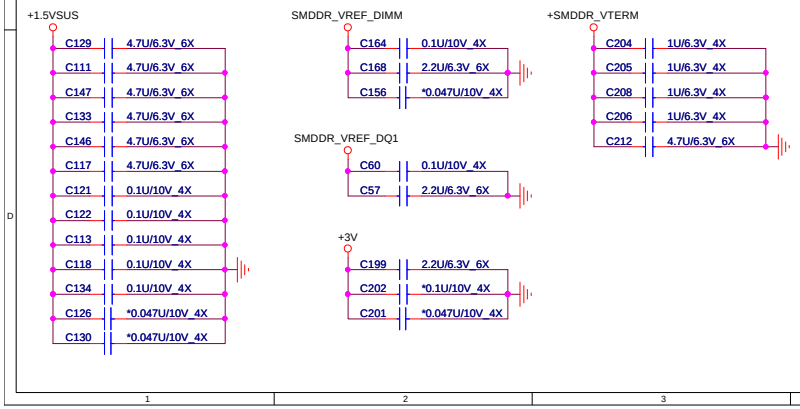
H=8

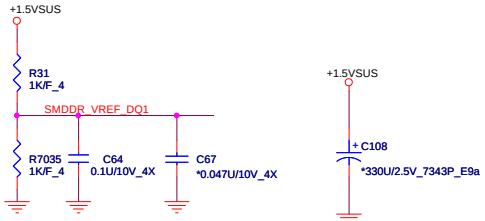


Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603

It can cost down 30%





Quanta Computer Inc.

PROJECT : TE4D

Size	Document Number	Rev
	DDR3 DIMM-1	A1A

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PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

~ 500mA

1600mA

12~16 mils width
110mA

12~16 mils width

GPU3500A
fcbga973-nvidia-n11p-es-a1
COMMON

PCI EXPRESS

B2A

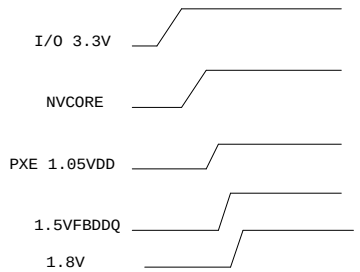
B2A

C3A

VGA HOLE

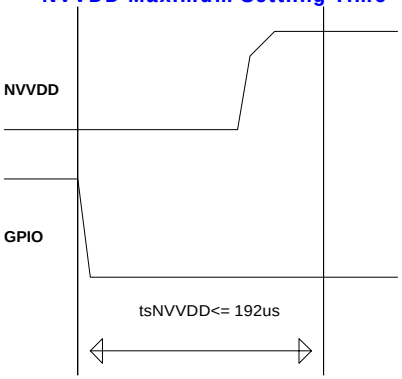
16-V

power up sequence

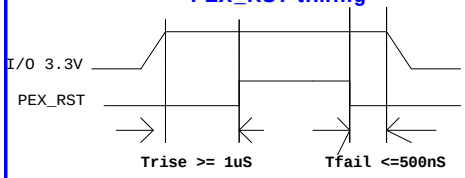


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



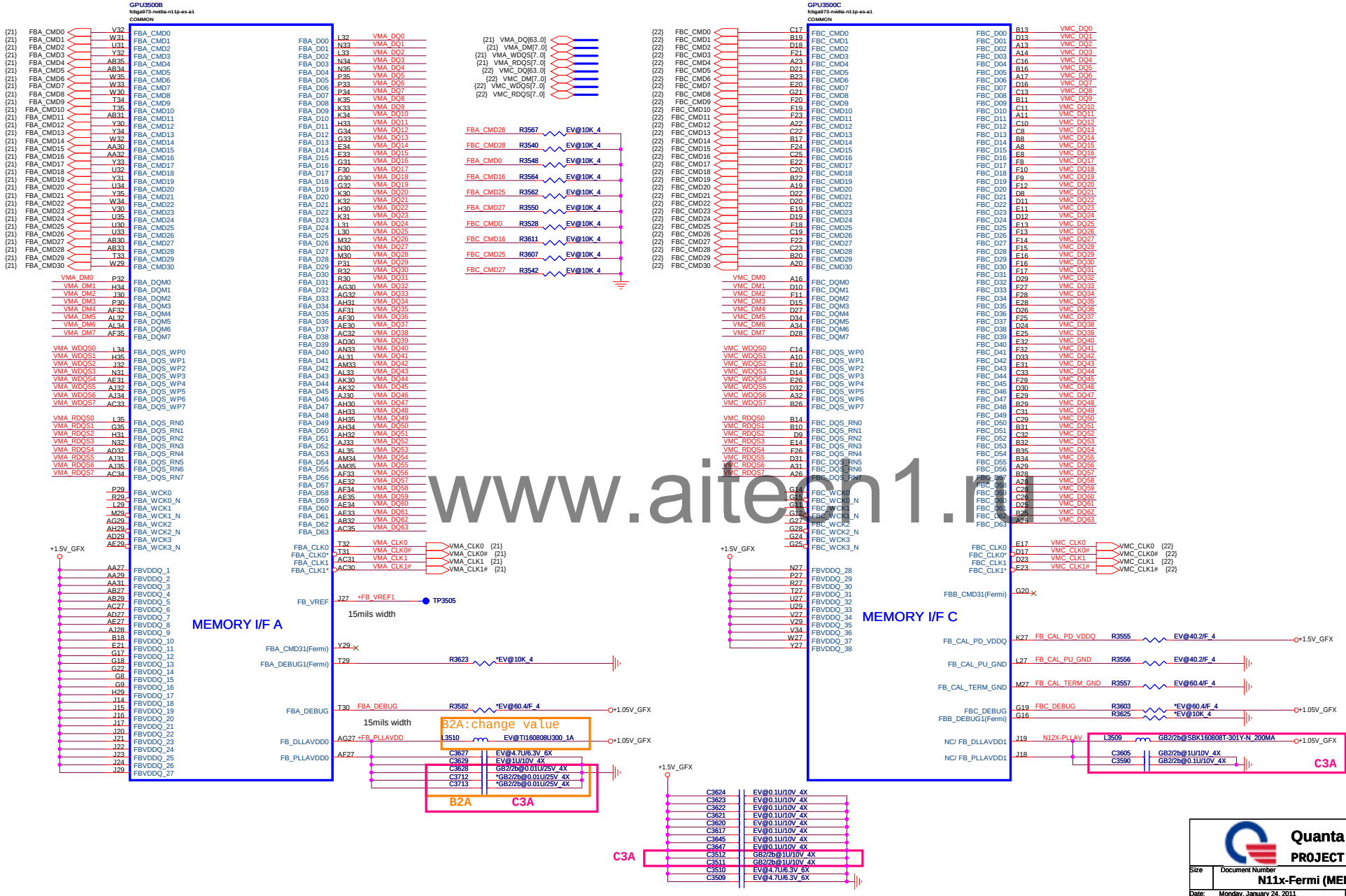
PEX_RST timing



Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	N11x-Fermi PCIE	1A

Date: Monday, January 24, 2011 Sheet 16 of 46



Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	N11x-Fermi (MEM I/F)	1A

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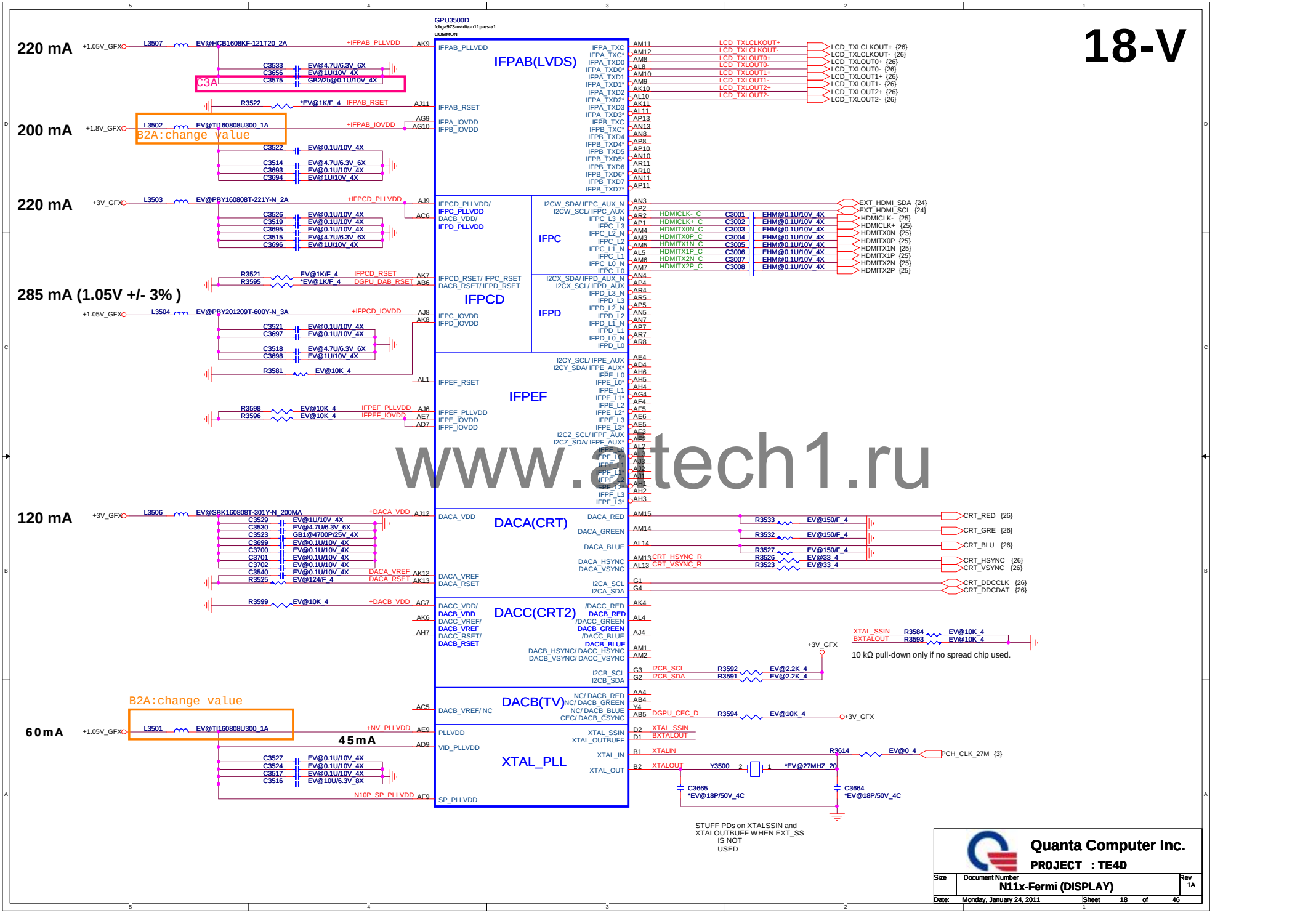
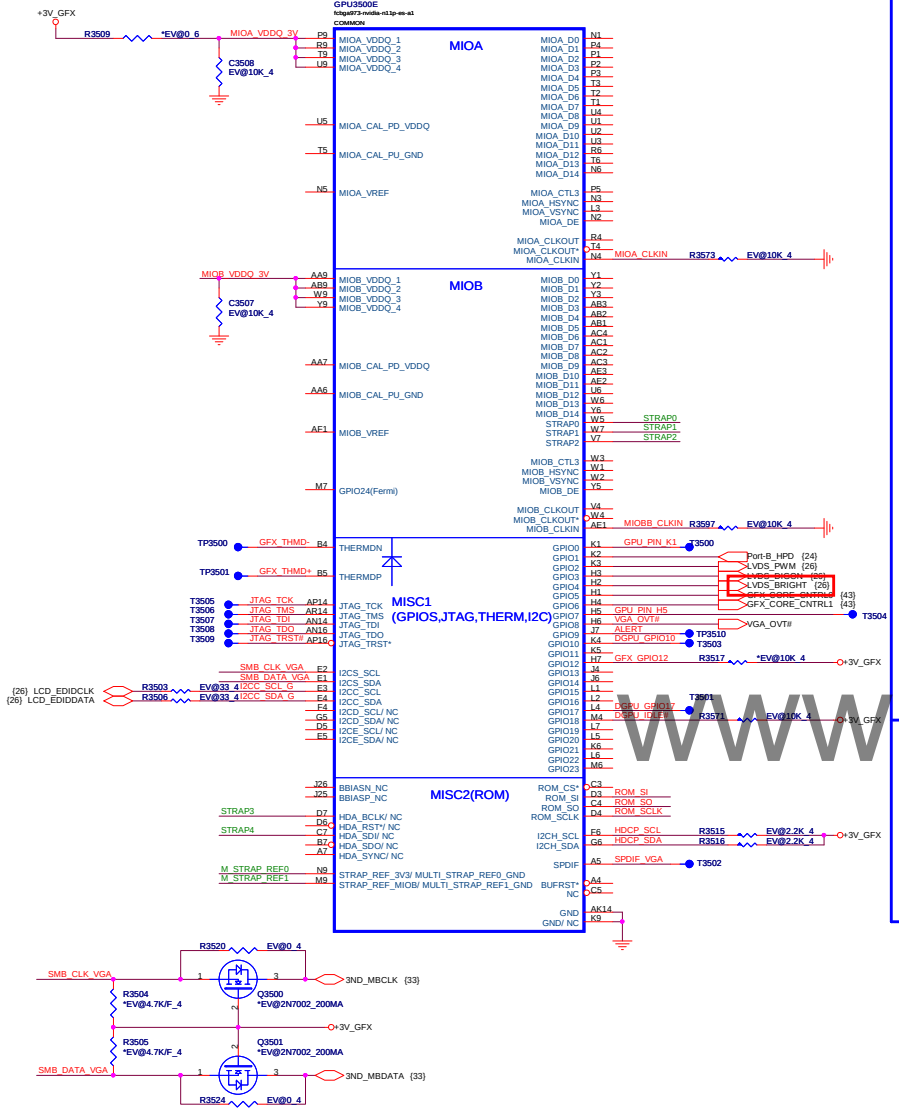
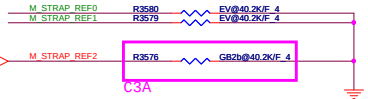


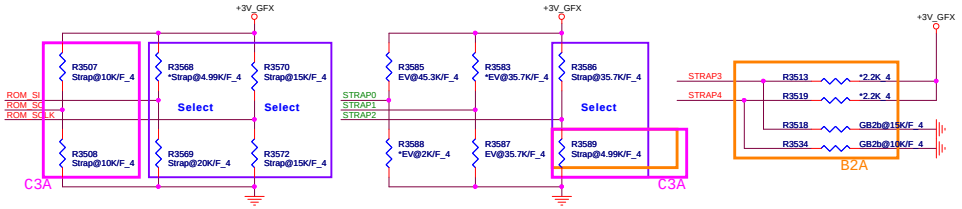


Strappin Model select

MODE	M_STRAP_REF0	M_STRAP_REF1	M_STRAP_REF2
Multi-level	40.2K/F_4 PD	40.2K/F_4 PD	40.2K/F_4 PD



MULTI level strap select



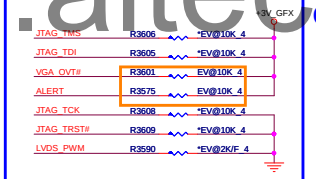
		Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12M-GE	N12P-GV	N12P-LP	
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010(15KPU)	1001(10KPU)	0010(15KPD)	
							PCI_DEVIDE[5]		
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	RAMCFG_T	RAMCFG_T	RAMCFG_T	
ROM_SO	GB1/2	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001(10KPD)		0001(10KPD)	
	GB2B	FB[1]	FB[0]				1001(10KPU)		Need to Update
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111(45KPU)	1111(45KPU)	1111(45KPU)	
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110(35KPD)	0110(35KPD)	0110(35KPD)	Need to Update
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1010(15KPU)	0000(5KPD)	1100(25KPU)	
STRAP3(Only GB2B)		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		0010(15KPD)		Need to Update
STRAP4(Only GB2B)		Reserve	Reserve	PCIE_MAX_SPEED	DP_PLL_VDD33V		0010(15KPD)		

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI	
0x0 0000					
0x1 0001					
0x2 0010	DDR3 64Mx16x8, 128bit, 1GB	Hynix	H5TQ1G63DFR-12C(800MHz) / H5TQ1G63DFR-11C(900MHz)		PD 15K
0x3 0011	DDR3 64Mx16x8, 128bit, 1GB	Samsung	K4W1G1646E-HC12(800MHz) / K4W1G1646E-HC11(900MHz)		PD 20K
0x4 0101					
0x5 0110					
0x6 0110	DDR3 128Mx16, 128bit, 1GB	Hynix	H5TQ2G63BFR-12C(800MHz) / H5TQ2G63BFR-11C(900MHz)		PD 35K
0x7 0111	DDR3 128Mx16, 128bit, 1GB	Samsung	K4W2G1646C-HC12(800MHz)2 / K4W2G1646C-HC11(900MHz)		PD 45K

N12M-GE(QS)
Device Id=0x0A7A
STRAP2 =15K PU
ROM_SCLK=15K PU

N12P-GV(QS)
Device Id=-x1050
STRAP2 =5K PD
ROM_SCLK=10K PU

N12P-LP(QS)
Device Id=0x0DEC
STRAP2=25K PU
ROM_SCLK=15K PD



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Quanta Computer Inc.
PROJECT : TE4D
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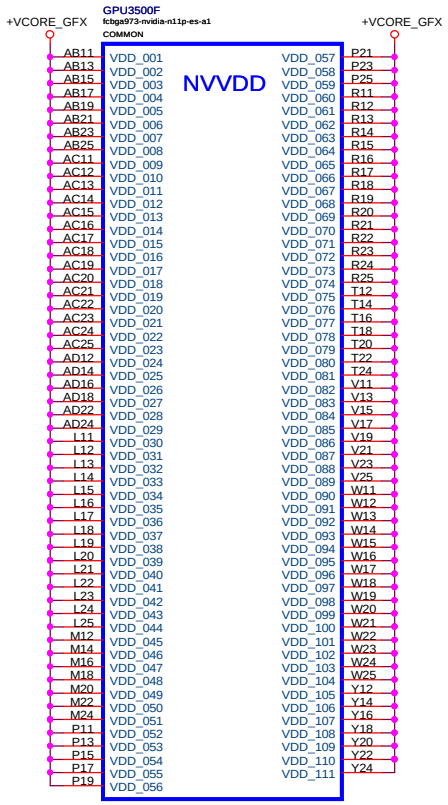
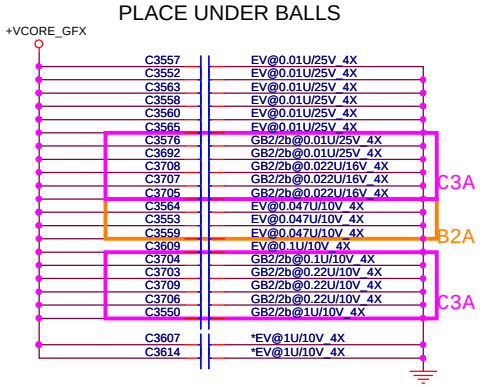
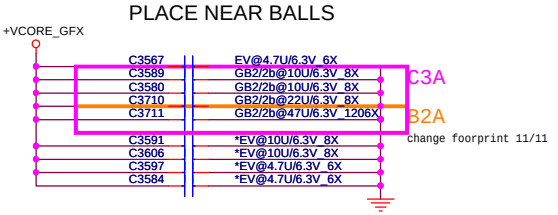
19-V

20-V







Quanta Computer Inc.		
PROJECT : TE4D		
Size	Document Number: N11x-Fermi (GND/Power)	Rev: 1A
Date: Monday, January 24, 2011	Sheet 20 of 46	

CHANNEL A: 256MB/512MB DDR3

{17} VMA_DQ[63..0]
{17} VMA_DM[7..0]
{17} VMA_WDQS[7..0]
{17} VMA_RDQS[7..0]

VRAM3502 — VMEM@VRAM _DDR3

VREFC_VMA1 M8 — VREFCA
VREFD_VMA1 H1 — VREFDQ

{17} FBA_CMD7 N3 — A0
{17} FBA_CMD20 P7 — A1
{17} FBA_CMD4 P3 — A2
{17} FBA_CMD14 N2 — A3
{17} FBA_CMD17 P8 — A4
{17} FBA_CMD6 P2 — A5
{17} FBA_CMD26 R8 — A6
{17} FBA_CMD3 R2 — A7
{17} FBA_CMD1 T8 — A8
{17} FBA_CMD10 R3 — A9
{17} FBA_CMD21 R7 — A10/AP
{17} FBA_CMD5 N7 — A11
{17} FBA_CMD22 T3 — A12/BC
{17} FBA_CMD18 T7 — A13
{17} FBA_CMD29 M7 — A14
{17} FBA_CMD30 — A15

{17} FBA_CMD12 M2 — BA0
{17} FBA_CMD9 N8 — BA1
{17} FBA_CMD13 M3 — BA2

{17} VMA_CLK0 J7 — CK
{17} VMA_CLK0# K7 — CK
{17} FBA_CMD0 K9 — CKE

{17} FBA_CMD25 K1 — ODT
{17} FBA_CMD2 L2 — CS
{17} FBA_CMD24 J3 — RAS
{17} FBA_CMD8 K3 — CAS
{17} FBA_CMD19 L3 — WE

VMA_WDQS2 F3 — DQSL
VMA_RDQS2 G3 — DQSL

VMA_DM2 E7 — DML
VMA_DM0 D3 — DMU

VMA_WDQS0 C7 — DQSU
VMA_RDQS0 B7 — DQSU

{17} FBA_CMD28 T2 — RESET

VMA_ZQ1 L8 — ZQ

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

DQL0 E3 — VMA_DQ21
DQL1 F7 — VMA_DQ18
DQL2 F2 — VMA_DQ22
DQL3 F8 — VMA_DQ19
DQL4 H3 — VMA_DQ20
DQL5 H8 — VMA_DQ17
DQL6 G2 — VMA_DQ23
DQL7 H7 — VMA_DQ16

DQU0 D7 — VMA_DQ1
DQU1 C3 — VMA_DQ7
DQU2 C8 — VMA_DQ3
DQU3 C2 — VMA_DQ6
DQU4 A7 — VMA_DQ0
DQU5 A2 — VMA_DQ5
DQU6 B8 — VMA_DQ2
DQU7 A3 — VMA_DQ4

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

+1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R3553 EV@243/F_4

VRAM3506 — VMEM@VRAM _DDR3

VREFC_VMA1 M8 — VREFCA
VREFD_VMA1 H1 — VREFDQ

FBA_CMD7 N3 — A0
FBA_CMD20 P7 — A1
FBA_CMD4 P3 — A2
FBA_CMD14 N2 — A3
FBA_CMD17 P8 — A4
FBA_CMD6 P2 — A5
FBA_CMD26 R8 — A6
FBA_CMD3 R2 — A7
FBA_CMD1 T8 — A8
FBA_CMD10 R3 — A9
FBA_CMD21 R7 — A10/AP
FBA_CMD5 N7 — A11
FBA_CMD22 T3 — A12/BC
FBA_CMD18 T7 — A13
FBA_CMD29 M7 — A14
FBA_CMD30 — A15

FBA_CMD12 M2 — BA0
FBA_CMD9 N8 — BA1
FBA_CMD13 M3 — BA2

VMA_CLK0 J7 — CK
VMA_CLK0# K7 — CK
FBA_CMD0 K9 — CKE

FBA_CMD25 K1 — ODT
FBA_CMD2 L2 — CS
FBA_CMD24 J3 — RAS
FBA_CMD8 K3 — CAS
FBA_CMD19 L3 — WE

VMA_WDQS3 F3 — DQSL
VMA_RDQS3 G3 — DQSL

VMA_DM3 E7 — DML
VMA_DM1 D3 — DMU

VMA_WDQS1 C7 — DQSU
VMA_RDQS1 B7 — DQSU

FBA_CMD28 T2 — RESET

VMA_ZQ2 L8 — ZQ

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

DQL0 E3 — VMA_DQ26
DQL1 F7 — VMA_DQ27
DQL2 F2 — VMA_DQ25
DQL3 F8 — VMA_DQ29
DQL4 H3 — VMA_DQ28
DQL5 H8 — VMA_DQ30
DQL6 G2 — VMA_DQ24
DQL7 H7 — VMA_DQ31

DQU0 D7 — VMA_DQ9
DQU1 C3 — VMA_DQ15
DQU2 C8 — VMA_DQ8
DQU3 C2 — VMA_DQ13
DQU4 A7 — VMA_DQ12
DQU5 A2 — VMA_DQ11
DQU6 B8 — VMA_DQ10
DQU7 A3 — VMA_DQ14

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

+1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R3612 EV@243/F_4

VRAM3503 — VMEM@VRAM _DDR3

VREFC_VMA3 M8 — VREFCA
VREFD_VMA3 H1 — VREFDQ

FBA_CMD22 N3 — A0
FBA_CMD4 P7 — A1
FBA_CMD20 P3 — A2
FBA_CMD9 N2 — A3
FBA_CMD6 P8 — A4
FBA_CMD17 P2 — A5
FBA_CMD3 R8 — A6
FBA_CMD26 R2 — A7
FBA_CMD1 T8 — A8
FBA_CMD5 R3 — A9
FBA_CMD19 L7 — A10/AP
FBA_CMD10 R7 — A11
FBA_CMD7 N7 — A12/BC
FBA_CMD29 T3 — A13
FBA_CMD18 T7 — A14
FBA_CMD13 M7 — A15

FBA_CMD12 M2 — BA0
FBA_CMD14 N8 — BA1
FBA_CMD30 M3 — BA2

{17} VMA_CLK1 J7 — CK
{17} VMA_CLK1# K7 — CK
{17} FBA_CMD27 K9 — CKE

{17} FBA_CMD16 K1 — ODT
FBA_CMD11 L2 — CS
FBA_CMD24 J3 — RAS
FBA_CMD8 K3 — CAS
FBA_CMD21 L3 — WE

VMA_WDQS4 F3 — DQSL
VMA_RDQS4 G3 — DQSL

VMA_DM4 E7 — DML
VMA_DM5 D3 — DMU

VMA_WDQS5 C7 — DQSU
VMA_RDQS5 B7 — DQSU

FBA_CMD28 T2 — RESET

VMA_ZQ3 L8 — ZQ

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

DQL0 E3 — VMA_DQ37
DQL1 F7 — VMA_DQ34
DQL2 F2 — VMA_DQ32
DQL3 F8 — VMA_DQ36
DQL4 H3 — VMA_DQ39
DQL5 H8 — VMA_DQ33
DQL6 G2 — VMA_DQ38
DQL7 H7 — VMA_DQ35

DQU0 D7 — VMA_DQ43
DQU1 C3 — VMA_DQ47
DQU2 C8 — VMA_DQ40
DQU3 C2 — VMA_DQ44
DQU4 A7 — VMA_DQ41
DQU5 A2 — VMA_DQ45
DQU6 B8 — VMA_DQ42
DQU7 A3 — VMA_DQ46

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

+1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

B2A

R3552 EV@243/F_4

VRAM3507 — VMEM@VRAM _DDR3

VREFC_VMA3 M8 — VREFCA
VREFD_VMA3 H1 — VREFDQ

FBA_CMD22 N3 — A0
FBA_CMD4 P7 — A1
FBA_CMD20 P3 — A2
FBA_CMD9 N2 — A3
FBA_CMD6 P8 — A4
FBA_CMD17 P2 — A5
FBA_CMD3 R8 — A6
FBA_CMD26 R2 — A7
FBA_CMD1 T8 — A8
FBA_CMD5 R3 — A9
FBA_CMD19 L7 — A10/AP
FBA_CMD10 R7 — A11
FBA_CMD7 N7 — A12/BC
FBA_CMD29 T3 — A13
FBA_CMD18 T7 — A14
FBA_CMD13 M7 — A15

FBA_CMD12 M2 — BA0
FBA_CMD14 N8 — BA1
FBA_CMD30 M3 — BA2

VMA_CLK1 J7 — CK
VMA_CLK1# K7 — CK
FBA_CMD27 K9 — CKE

FBA_CMD16 K1 — ODT
FBA_CMD11 L2 — CS
FBA_CMD24 J3 — RAS
FBA_CMD8 K3 — CAS
FBA_CMD21 L3 — WE

VMA_WDQS7 F3 — DQSL
VMA_RDQS7 G3 — DQSL

VMA_DM7 E7 — DML
VMA_DM6 D3 — DMU

VMA_WDQS6 C7 — DQSU
VMA_RDQS6 B7 — DQSU

FBA_CMD28 T2 — RESET

VMA_ZQ4 L8 — ZQ

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

DQL0 E3 — VMA_DQ60
DQL1 F7 — VMA_DQ62
DQL2 F2 — VMA_DQ59
DQL3 F8 — VMA_DQ58
DQL4 H3 — VMA_DQ63
DQL5 H8 — VMA_DQ56
DQL6 G2 — VMA_DQ61
DQL7 H7 — VMA_DQ57

DQU0 D7 — VMA_DQ48
DQU1 C3 — VMA_DQ53
DQU2 C8 — VMA_DQ50
DQU3 C2 — VMA_DQ52
DQU4 A7 — VMA_DQ51
DQU5 A2 — VMA_DQ54
DQU6 B8 — VMA_DQ49
DQU7 A3 — VMA_DQ55

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

+1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

B2A

R3613 EV@243/F_4

VMA_CLK0
R3549 EV@160/F_4
VMA_CLK0#

+1.5V_GFX
R3566 EV@1.33K/F_4
VREFC_VMA1
R3565 EV@1.33K/F_4
C3643 EV@0.1U/10V_4X

+1.5V_GFX
R3560 EV@1.33K/F_4
VREFD_VMA1
R3558 EV@1.33K/F_4
C3641 EV@0.1U/10V_4X

{17} FBA_CMD15 — FBA_CMD15 — TP3506
{17} FBA_CMD23 — FBA_CMD23 — TP3507

VMA_CLK1
R3551 EV@160/F_4
VMA_CLK1#

+1.5V_GFX
R3563 EV@1.33K/F_4
VREFC_VMA3
R3561 EV@1.33K/F_4
C3642 EV@0.1U/10V_4X

+1.5V_GFX
R3559 EV@1.33K/F_4
VREFD_VMA3
R3554 EV@1.33K/F_4
C3640 EV@0.1U/10V_4X

+1.5V_GFX
C3687 C@10U/6.3V_8X
C3588 EV@0.1U/10V_4X
C3638 EV@0.1U/10V_4X
C3683 EV@0.1U/10V_4X
C3676 EV@0.1U/10V_4X
C3680 EV@0.1U/10V_4X
C3689 EV@0.1U/10V_4X

+1.5V_GFX
C3646 EV@10U/6.3V_8X
C3654 EV@0.1U/10V_4X
C3655 EV@0.1U/10V_4X
C3639 EV@0.1U/10V_4X
C3691 EV@0.1U/10V_4X
C3652 EV@0.1U/10V_4X
C3648 EV@0.1U/10V_4X

+1.5V_GFX
C3671 EV@10U/6.3V_8X
C3673 EV@0.1U/10V_4X
C3653 EV@0.1U/10V_4X
C3644 EV@0.1U/10V_4X
C3649 EV@0.1U/10V_4X
C3650 EV@0.1U/10V_4X
C3593 EV@0.1U/10V_4X

+1.5V_GFX
C3661 C@10U/6.3V_8X
C3685 EV@0.1U/10V_4X
C3690 EV@0.1U/10V_4X
C3679 EV@0.1U/10V_4X
C3682 EV@0.1U/10V_4X
C3675 EV@0.1U/10V_4X
C3681 EV@0.1U/10V_4X

Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	N11x-Fermi VRAM A	1A
Date: Monday, January 24, 2011	Sheet 21 of 46	

CHANNEL B: 256MB/512MB DDR3

{17} VMC_DQ[63..0]
{17} VMC_DM[7..0]
{17} VMC_WDQS[7..0]
{17} VMC_RDQS[7..0]

VRAM3504 / VRAM3500 / VRAM3501 / VRAM3505

Should be 240 Ohms +-1%

R3574 GB2@243/F_4
R3530 GB2@243/F_4
R3543 GB2@243/F_4
R3610 GB2@243/F_4

96-BALL SDRAM DDR3
GB2@VRAM _DDR3

+1.5V_GFX

R3510 GB2@160/F_4
R3578 GB2@1.33K/F_4
R3577 GB2@1.33K/F_4
C3658 GB2@0.1U/10V_4X
R3529 GB2@1.33K/F_4
R3531 GB2@1.33K/F_4
C3547 GB2@0.1U/10V_4X
R3541 GB2@160/F_4
R3545 GB2@1.33K/F_4
R3544 GB2@1.33K/F_4
C3637 GB2@0.1U/10V_4X
R3537 GB2@1.33K/F_4
R3536 GB2@1.33K/F_4
C3566 GB2@0.1U/10V_4X

TP3504
TP3503

C3651 C@10U/6.3V_8X
C3678 GB2@0.1U/10V_4X
C3538 GB2@0.1U/10V_4X
C3670 GB2@0.1U/10V_4X
C3659 GB2@0.1U/10V_4X
C3666 GB2@0.1U/10V_4X
C3684 GB2@0.1U/10V_4X

C3548 GB2@10U/6.3V_8X
C3594 GB2@0.1U/10V_4X
C3542 GB2@0.1U/10V_4X
C3662 GB2@0.1U/10V_4X
C3657 GB2@0.1U/10V_4X
C3663 GB2@0.1U/10V_4X
C3667 GB2@0.1U/10V_4X

C3669 GB2@10U/6.3V_8X
C3577 GB2@0.1U/10V_4X
C3686 GB2@0.1U/10V_4X
C3688 GB2@0.1U/10V_4X
C3578 GB2@0.1U/10V_4X
C3549 GB2@0.1U/10V_4X
C3528 GB2@0.1U/10V_4X

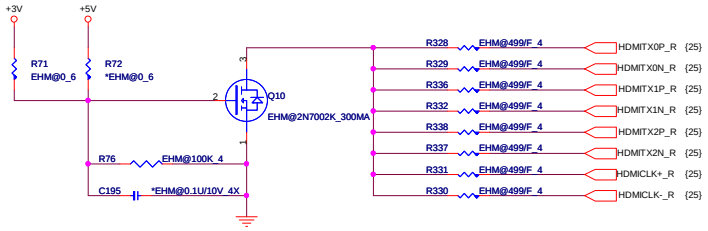
C3573 C@10U/6.3V_8X
C3579 GB2@0.1U/10V_4X
C3635 GB2@0.1U/10V_4X
C3633 GB2@0.1U/10V_4X
C3634 GB2@0.1U/10V_4X
C3636 GB2@0.1U/10V_4X
C3537 GB2@0.1U/10V_4X

Quanta Computer Inc.
PROJECT : TE4D

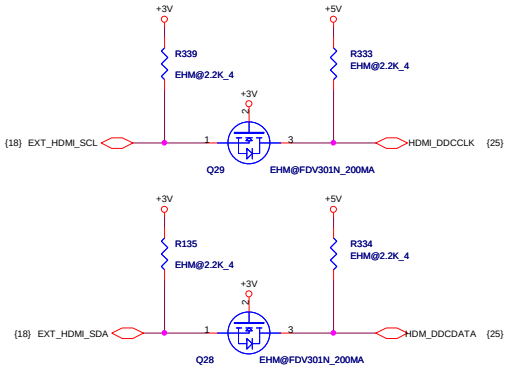
Size	Document Number	Rev
	N11x-Fermi VRAM B	1A
Date: Monday, January 24, 2011	Sheet 22 of 46	

HDMI LEVEL SHIFT (VGA)

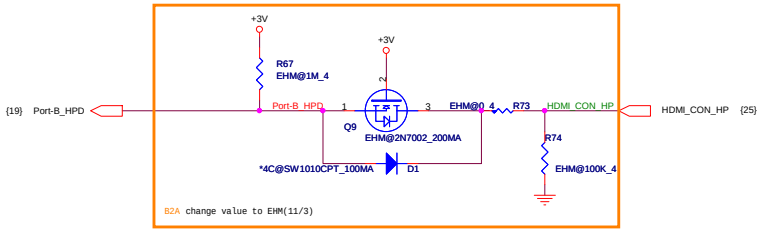
[HDM]



HDMI SMBUS (VGA)



Hot Plug Detector (VGA)



24

LVDS (VGA)

CRT (VGA)

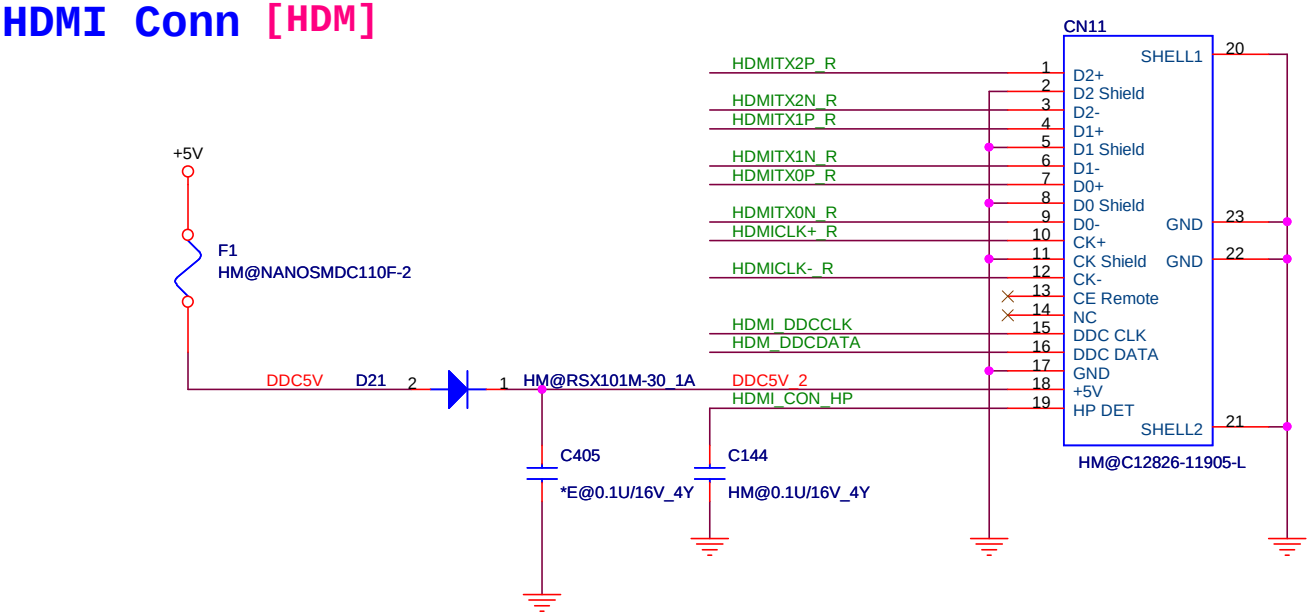
Quanta Computer Inc.

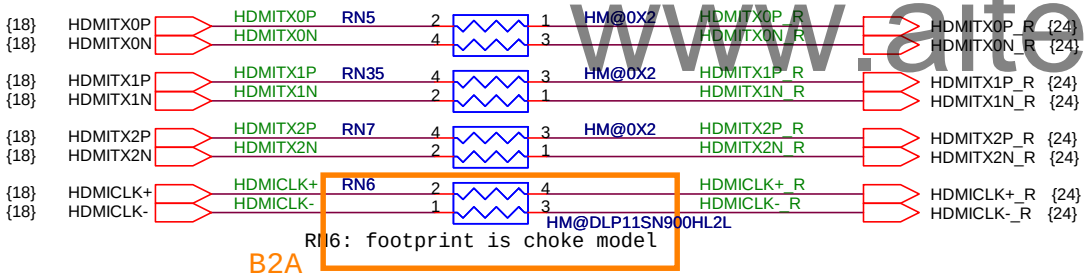
PROJECT : TE4D

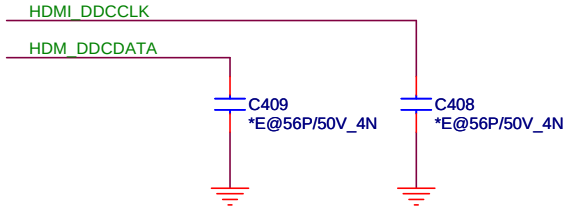
Size	Document Number	Rev
	VGA	A1A

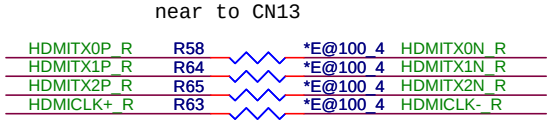
Date: Monday, January 24, 2011 Sheet 24 of 46

HDMI Conn [HDM]









B2A EMI

此組之後可以刪掉，重覆到了

Quanta Computer Inc.		
PROJECT : TE4D		
Size	Document Number: HDMI CONN	Rev: A1A
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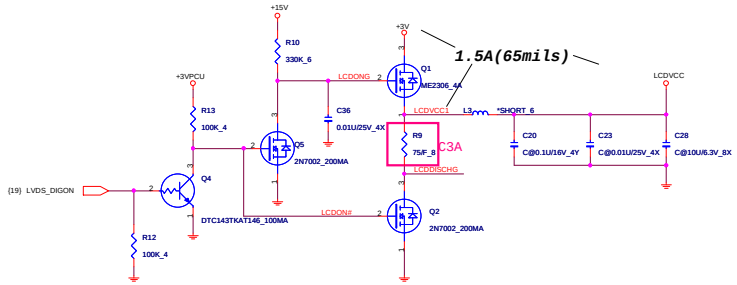
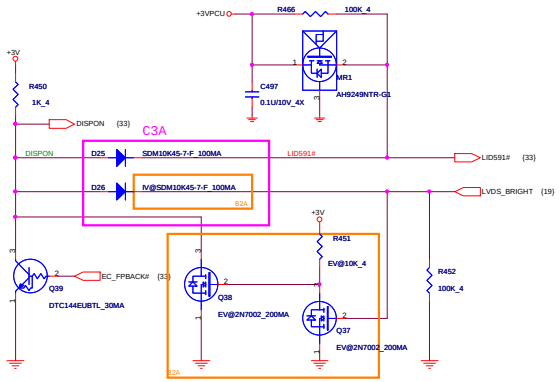
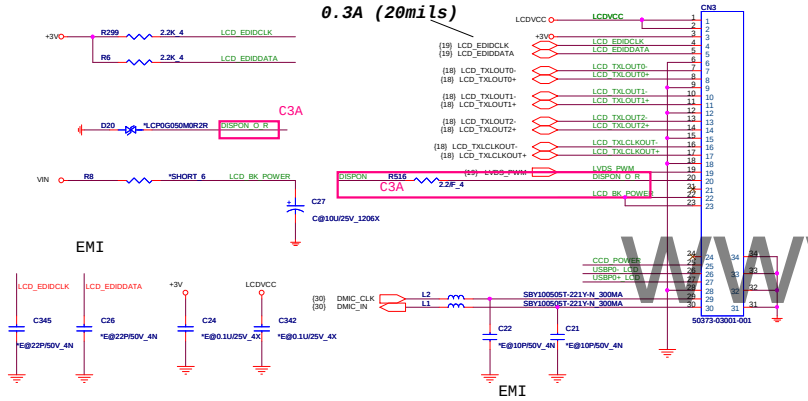
LCD POWER SWITCH
<LDS>



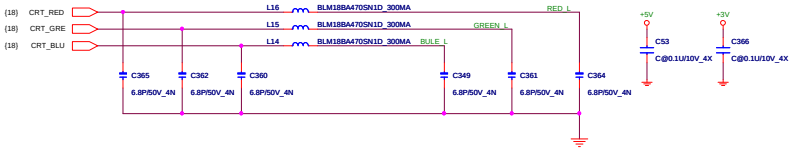
HALL Sensor
<HSR>



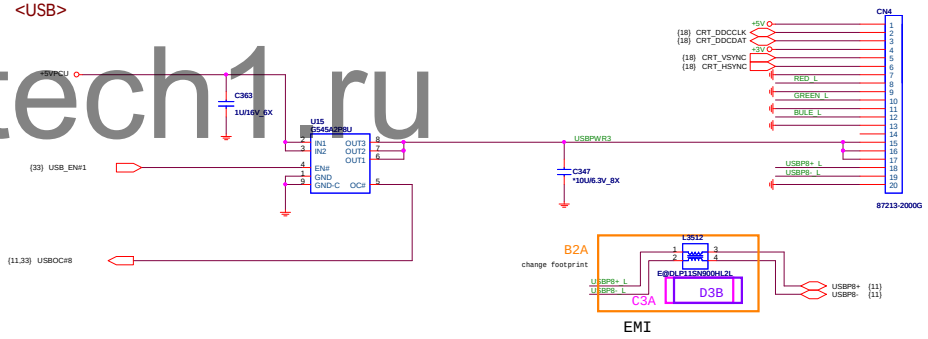
LCD Panel Module
[LDS]



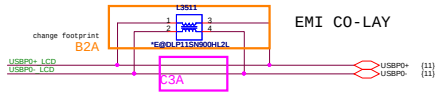
CRT
<CRT>

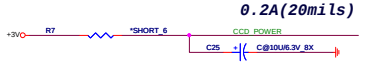


USB for CRT BOARD (Right)
<USB>



CCD
[CCD]





Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	LCD/LED Panel/CCD	A1A
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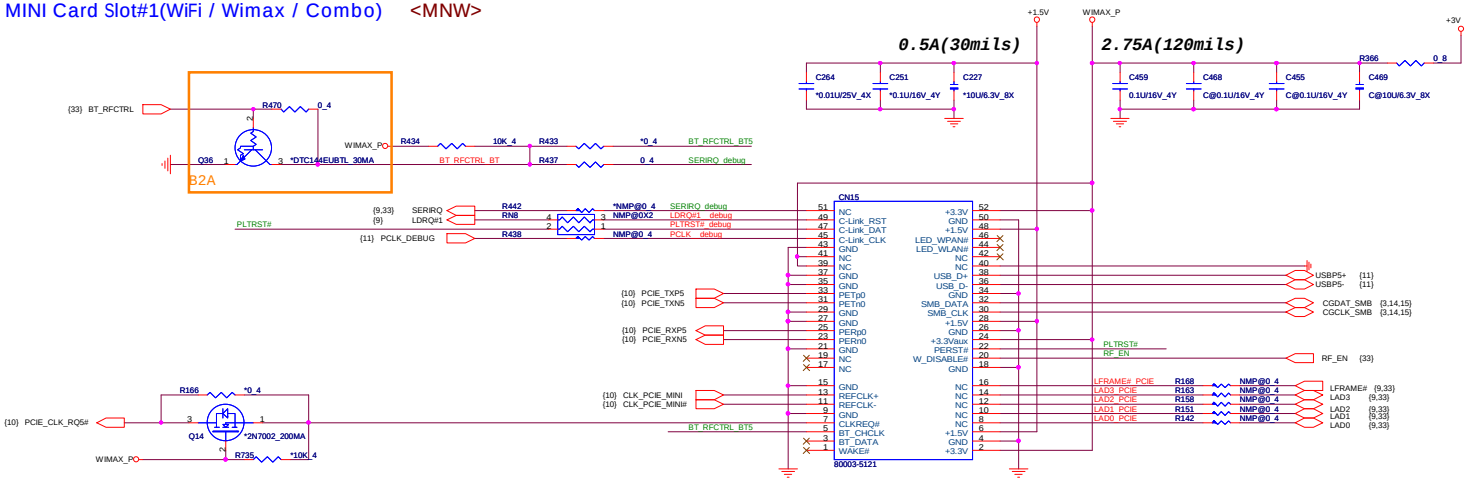
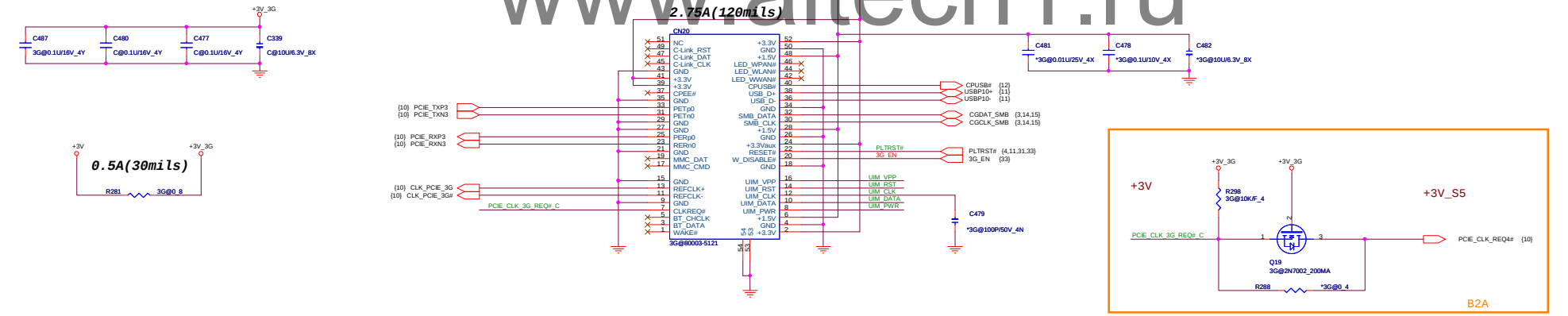
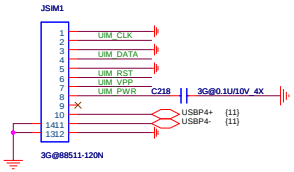
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



MINI Card Slot#2-3G <MNT>



SIM CARD



Quanta Computer Inc.
PROJECT : TE4D
Size | Document Number: MINI CARD(WLAN/3G/SIM Card) | Rev: A1A
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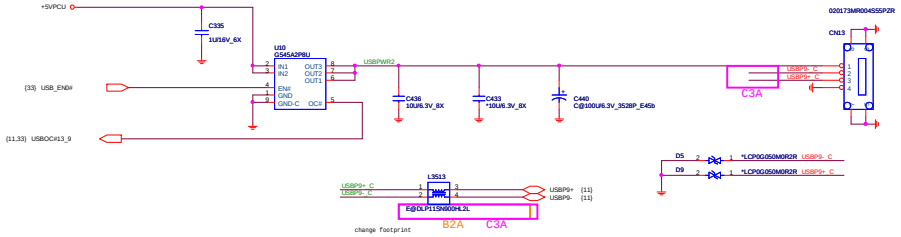
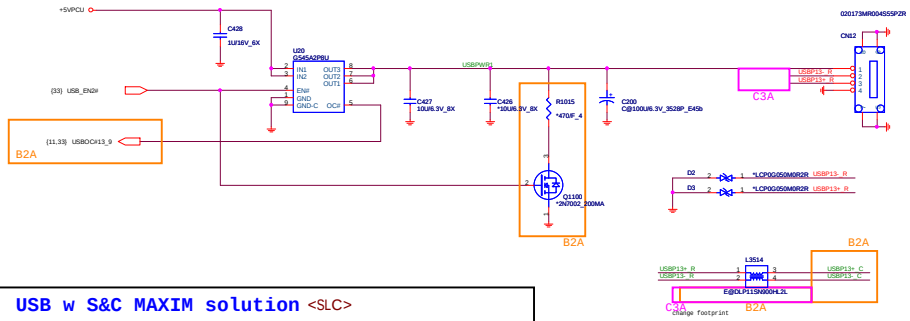
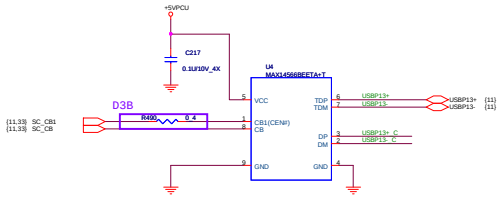
USB2.0 MB SIDE (Left) 1 <USB>



USB2.0 MB SIDE (Left) 2 <USB>

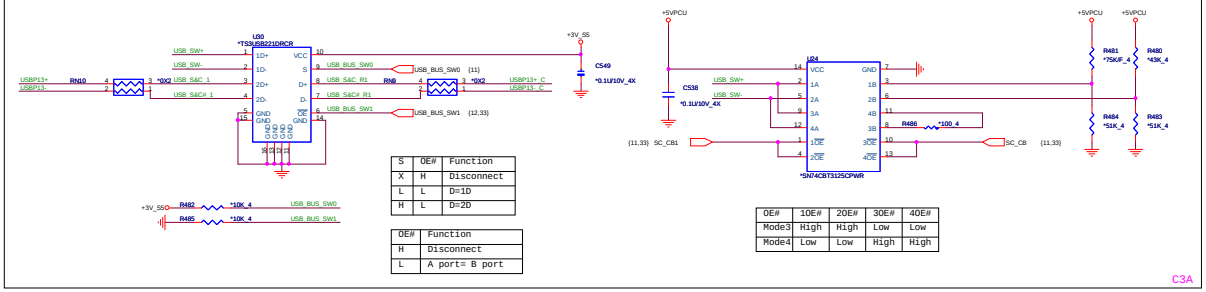


USB w S&C MAXIM solution <SLC>



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

USB w S&C TI solution <SLC>



S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

OE#	Function
H	Disconnect
L	A port= B port

OE#	1OE#	2OE#	3OE#	4OE#
Mode3	High	High	Low	Low
Mode4	Low	Low	High	High

Quanta Computer Inc.
PROJECT : TE4D
Size | Document Number: TP/SW/ESATA/USB+Audio/LED | Rev: A1A
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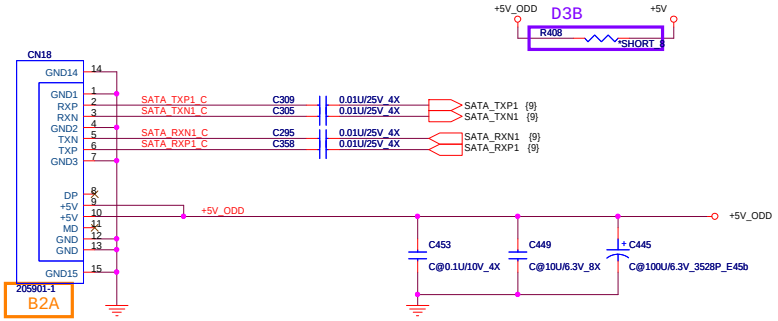
SATA ODD

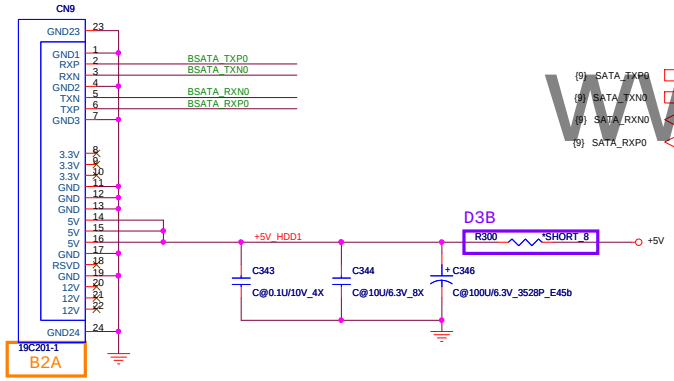
[ODD]



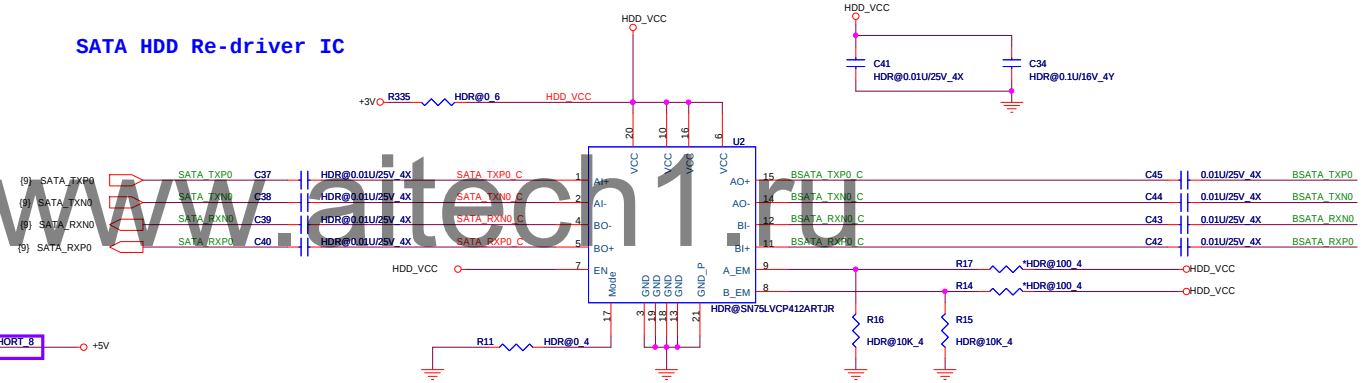
ODD Zero power . (Only for Intel)<OZP>

SATA HDD

[HDD]

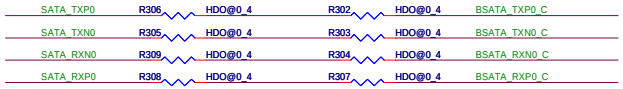


SATA HDD Re-driver IC



SATA Re-driver Bypass

Colay with Redriver IC



Quanta Computer Inc.

PROJECT : TE4D

Size	Document Number	Rev
	HDD/ODD/MDC	A1A

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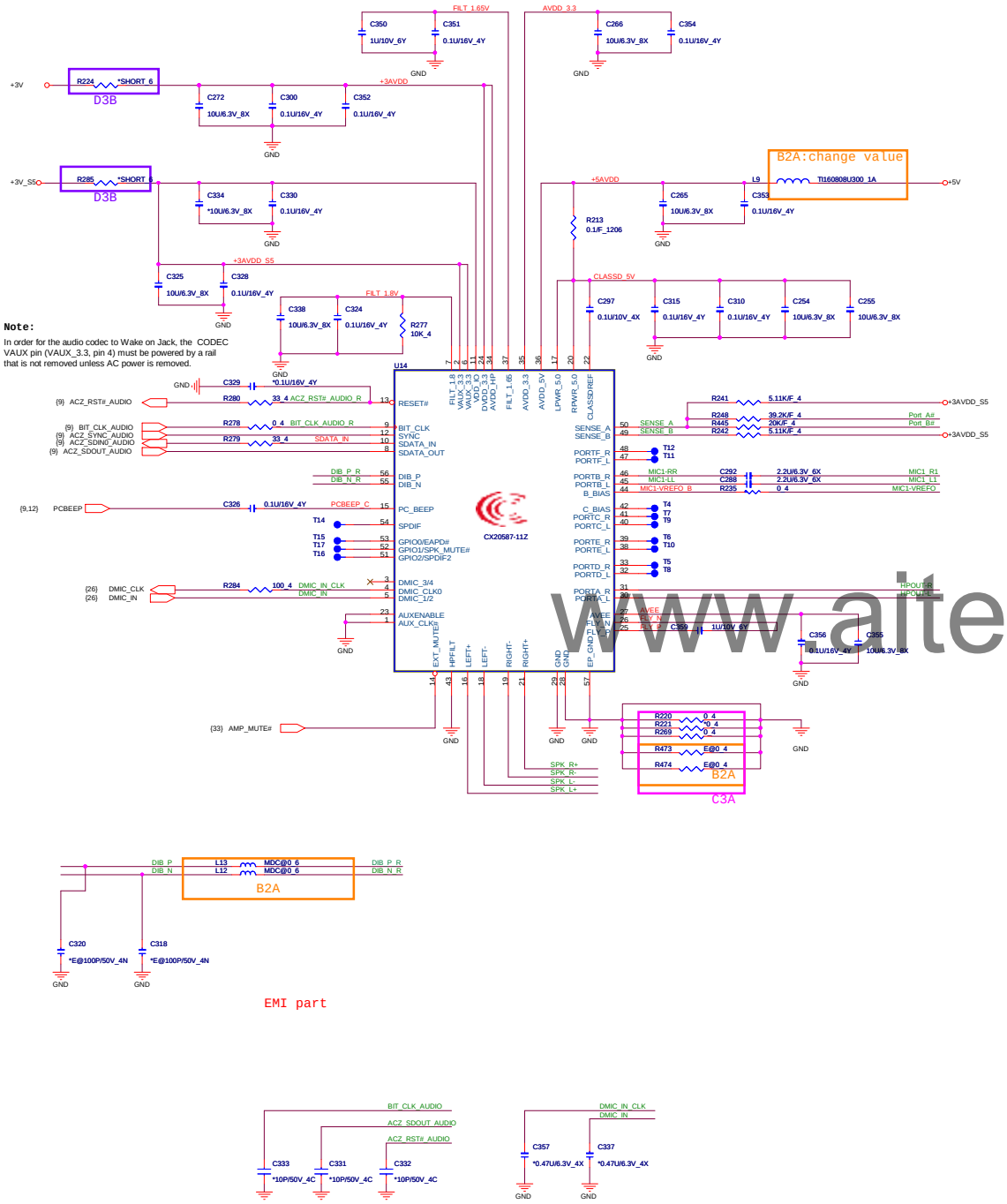
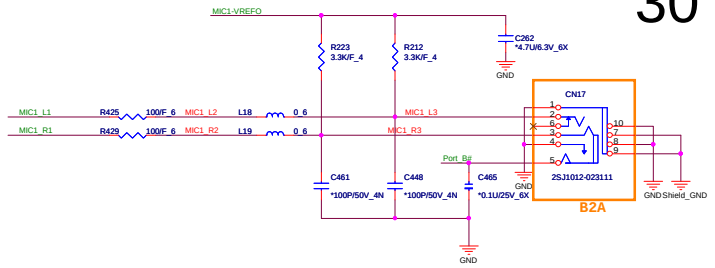
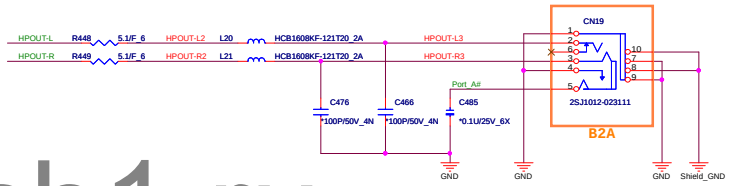
Codec(CX20587-11Z) <ADO/MDC/AMP>



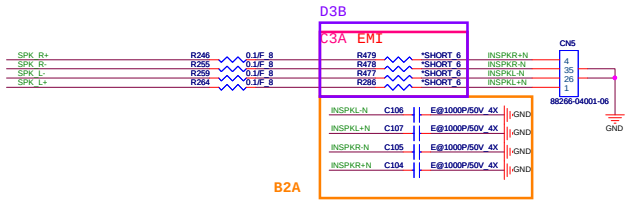
EXT MIC <ADO/AMP>



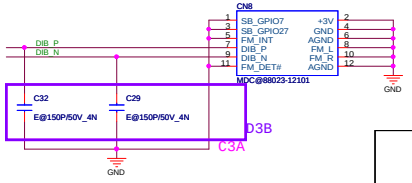
EXT H.P / Beats <ADO/AMP>



INT SPK <ADO/AMP>



MDC <MDC>



Quanta Computer Inc.
PROJECT : TE4D

Size	Document Number	Rev
	Codec (CX20587)	A1A
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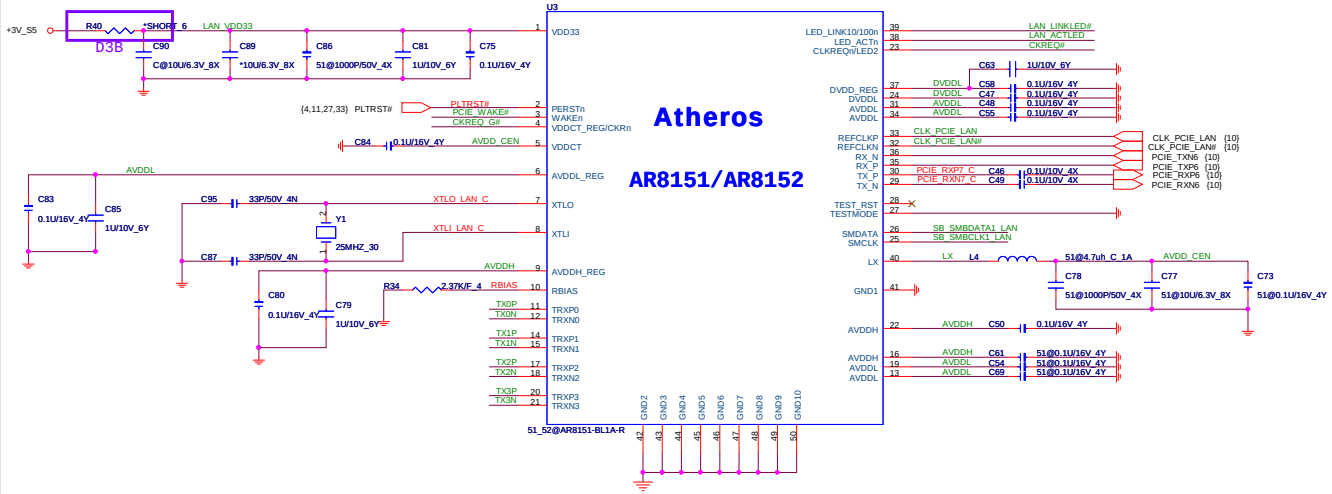
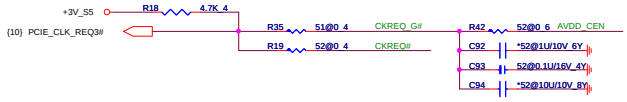
Atheros Lan <LAN/LN1/LNG>



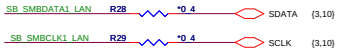
GIGA:AR8151-BL1A-R = AL008151005

10/100:AR8152-BL1A-R = AL008152009



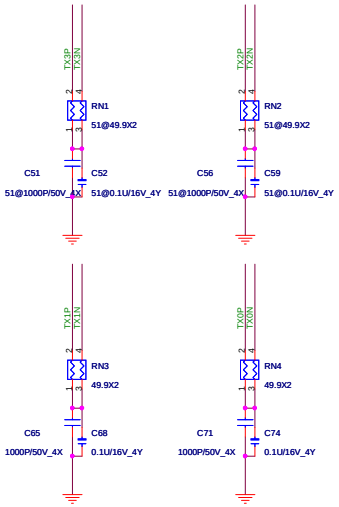
LAN-Wake up function<LAN>

LAN-SM-Bus <LAN>

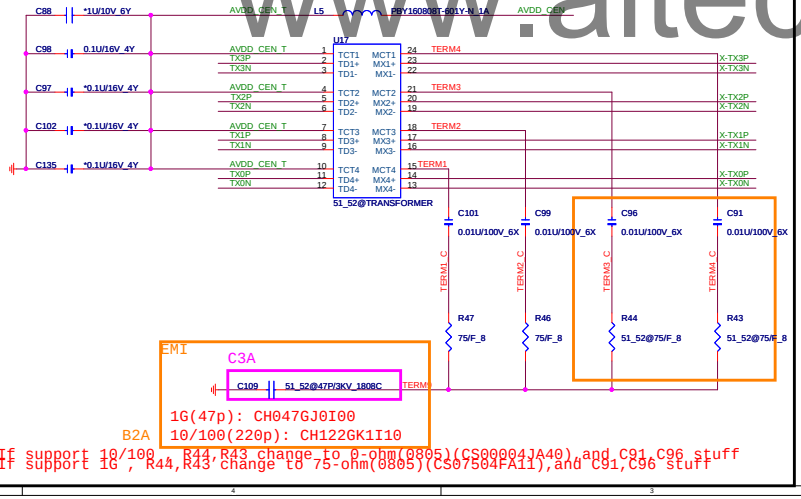


LAN-terminator<LAN/LN1/LNG>

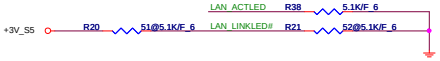
PLACE NEAR LAN IC SIDE



LAN-Transformer <LAN/LN1/LNG>

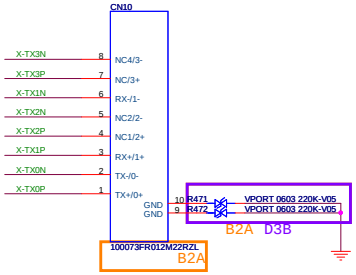


LAN-Strap function <LAN/LN1/LNG>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

LAN(RJ45)-CONN Interface <LAN>



Quanta Computer Inc.

PROJECT : TE4D

Size	Document Number	Rev
	Atheros Lan	A1A

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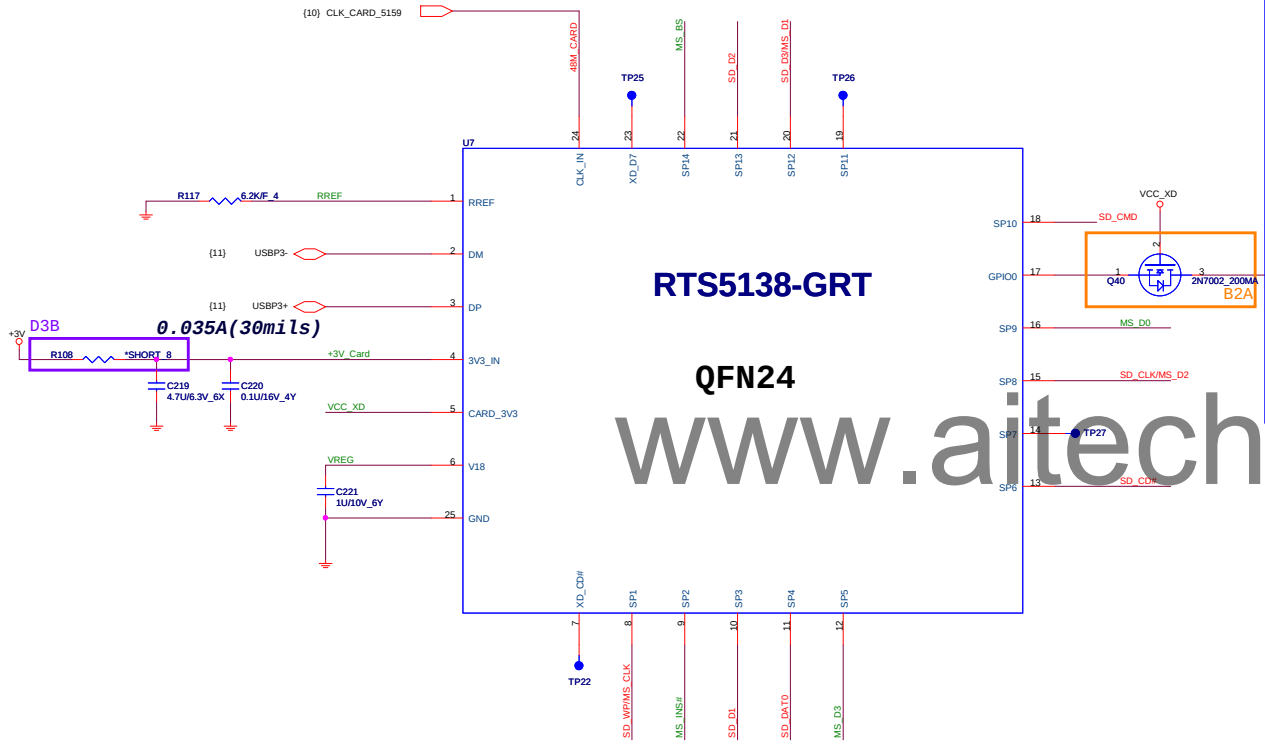
3 IN 1 CARD READER

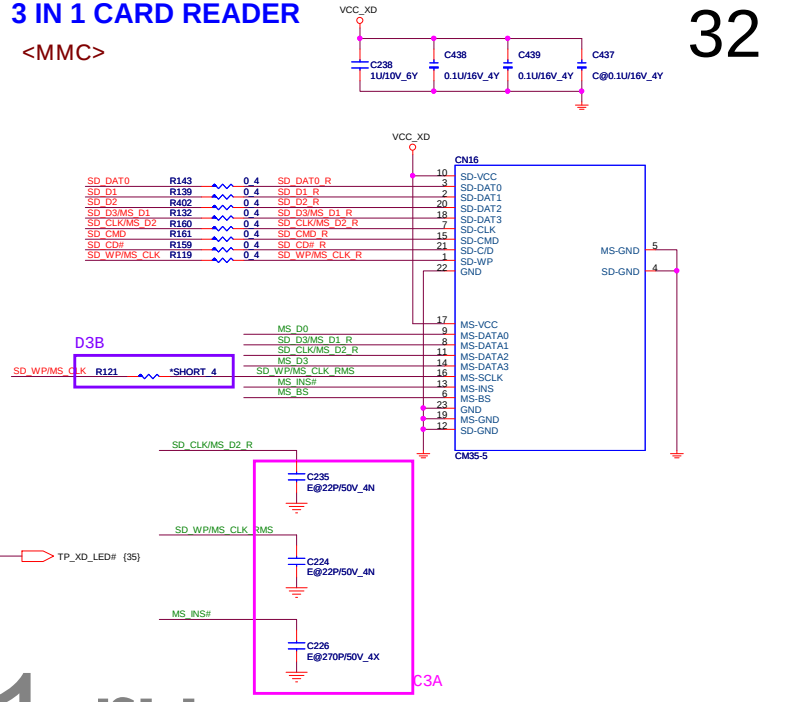
Card reader controller <MMC>



3 IN 1 CARD READER

<MMC>

32



Quanta Computer Inc.		
PROJECT : TE4D		
Size	Document Number: RTS5138 (Card Reader)	Rev: A1A
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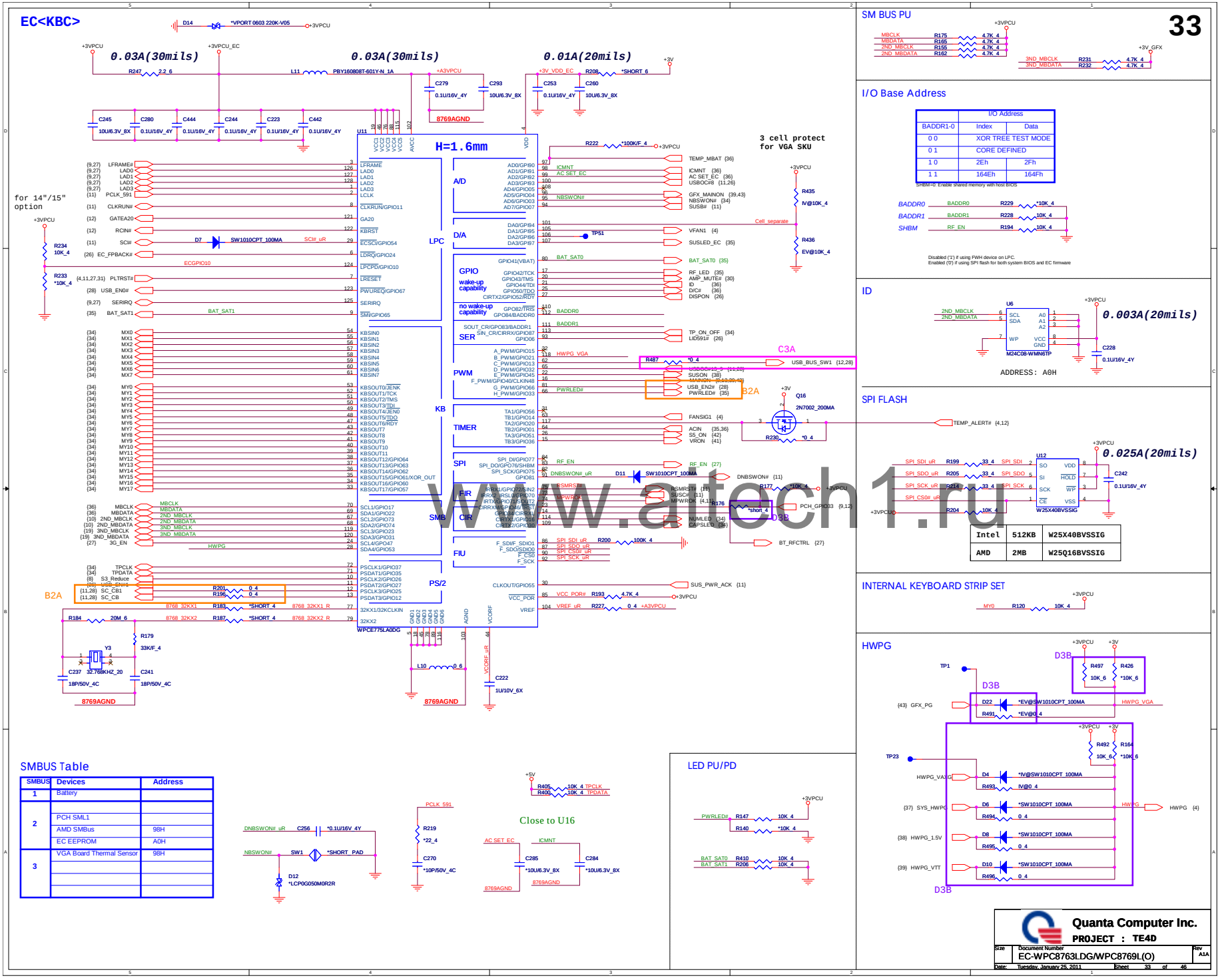
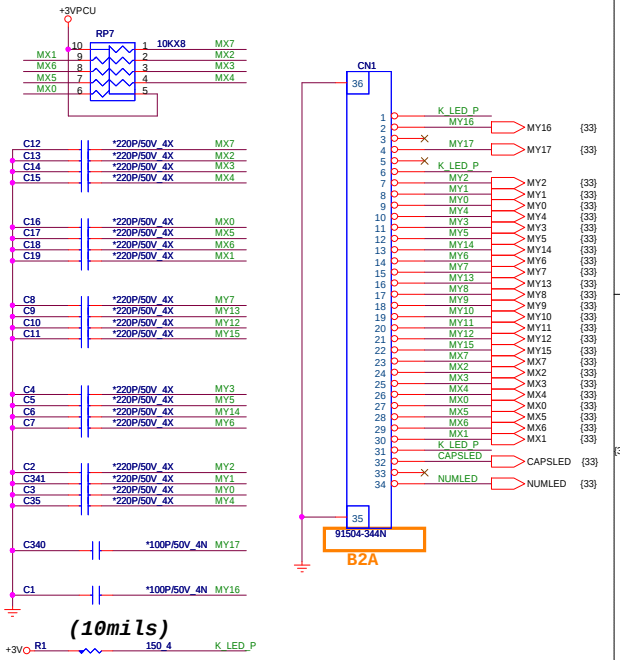
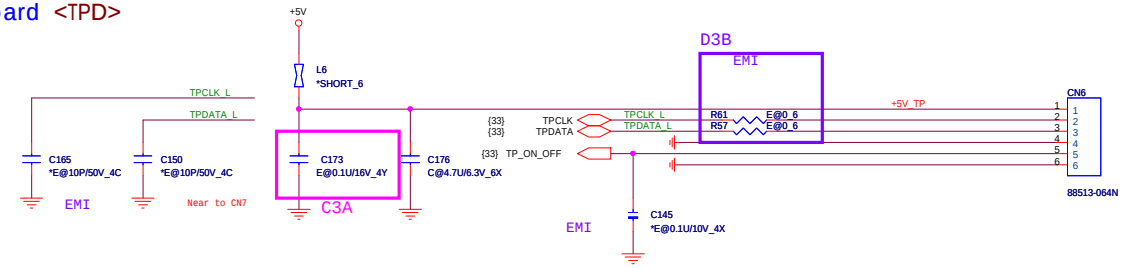


INT KeyBoard <KBC>



TP board <TPD>



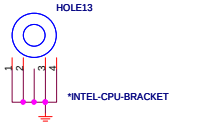
Power board <PSW>

K/B LED power <KBP>

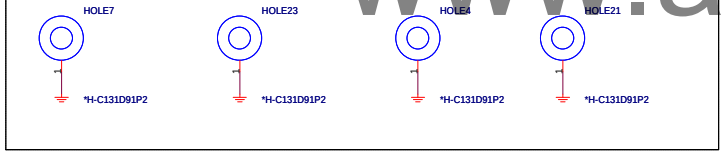
Only for Huron River

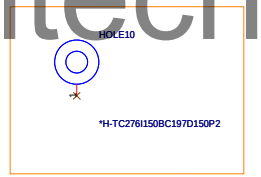
HOLE

CPU



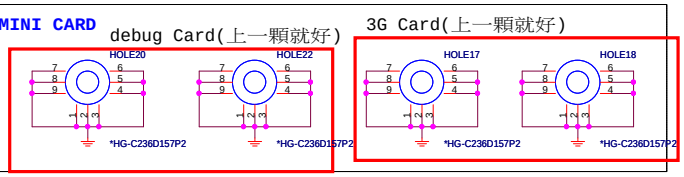
HDD&ODD



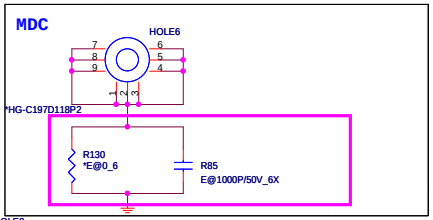


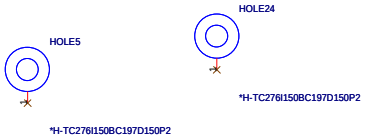
MINI CARD

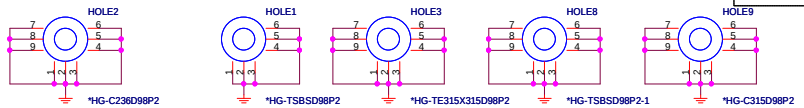
debug Card(上一顆就好)　3G Card(上一顆就好)

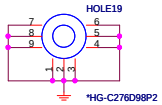


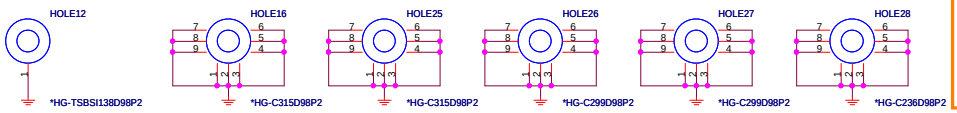
MDC

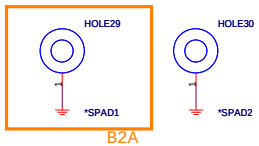












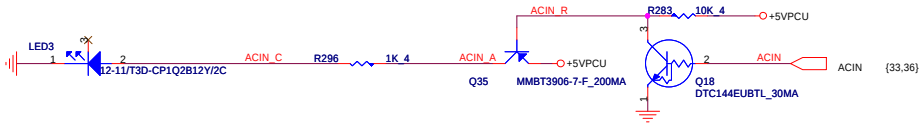
B2A

Quanta Computer Inc.
PROJECT : TE4D

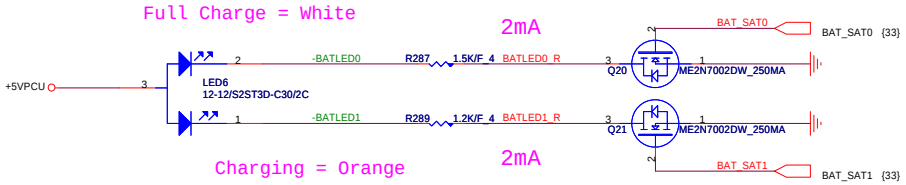
Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	A1A
Date: Monday, January 24, 2011	Sheet 34 of 46	

LED

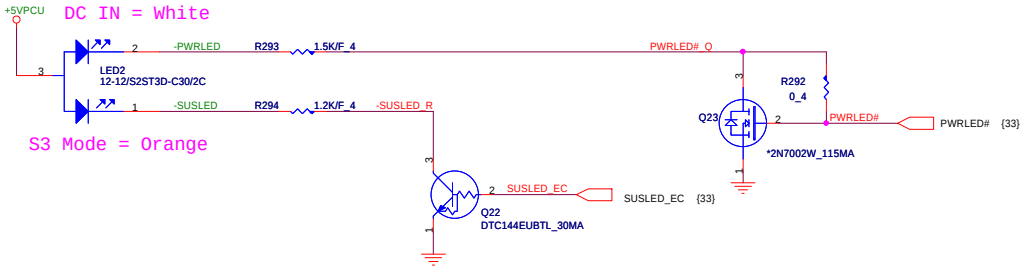
AC-IN



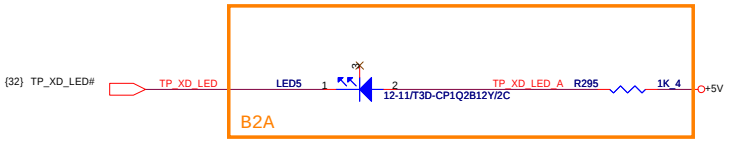
BATERRY



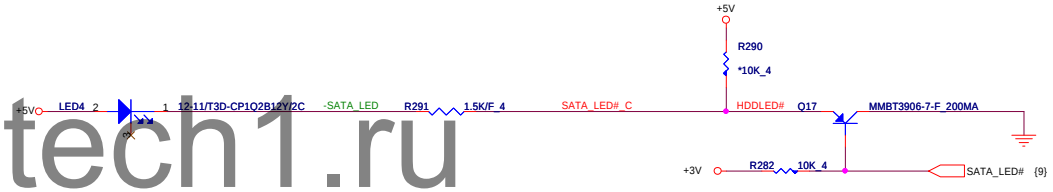
POWER



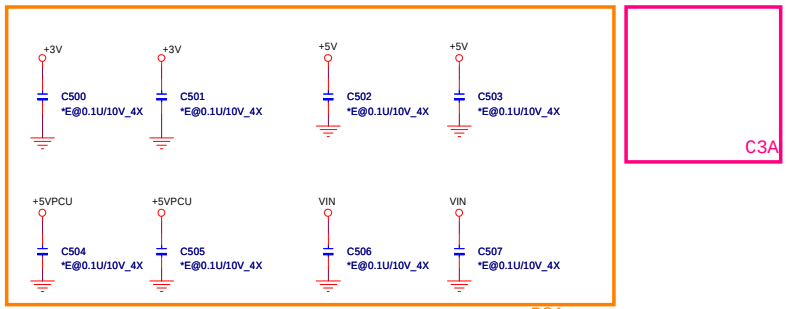
CARDREADER



HDD/ODD



RF LED

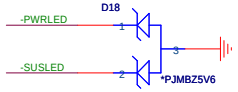


EMI

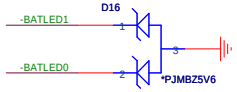
C3A

ESD Protect

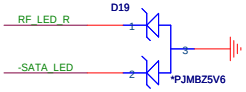
FOR POWER LED



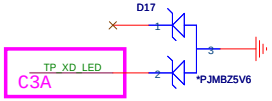
FOR BATTERY LED



FOR HDD/RF LED



FOR CARDREADER LED

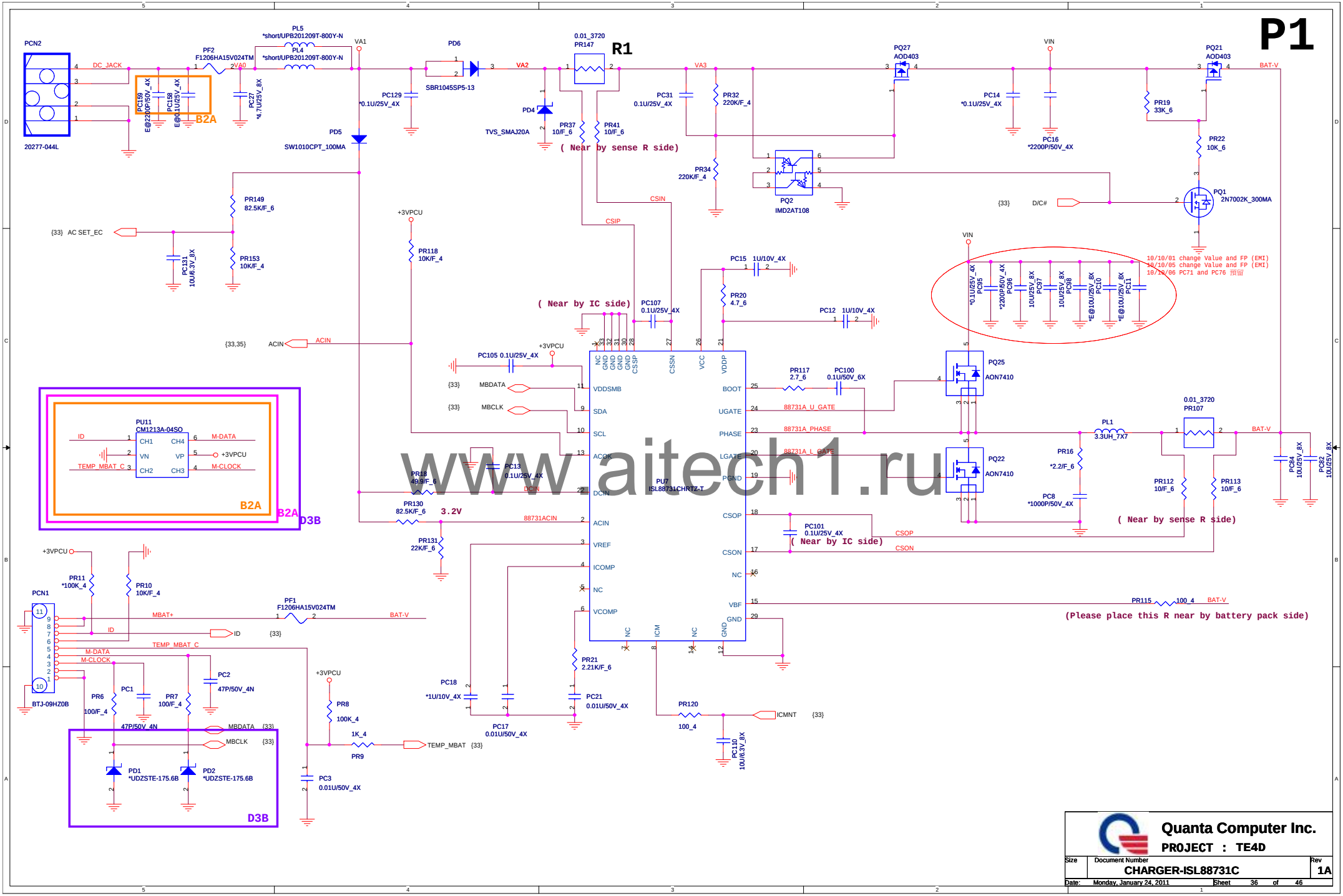


Quanta Computer Inc.

PROJECT : TE4D

Size	Document Number	Rev
	LED	A1A

Date: Monday, January 24, 2011 Sheet 35 of 46


P1
R1
PCN2
20277-044L
DC_JACK
PF2
F1206HA15V024TM
PL5
*short/UPB201209T-800Y-N
PL4
*short/UPB201209T-800Y-N
VA1
VA2
VA3
PD6
SBR1045SP5-13
PD4
TVS_SMAJ20A
PD5
SW1010CPT_100MA
0.01_3720
PR147
PR37
10/F_6
PR41
10/F_6
(Near by sense R side)
PC31
0.1U/25V_4X
PR32
220K/F_4
PR34
220K/F_4
PQ27
AOD403
PQ2
IMD2AT108
VIN
PC14
*0.1U/25V_4X
PC16
*2200P/50V_4X
PQ21
AOD403
BAT-V
PR19
33K_6
PR22
10K_6
PQ1
2N7002K_300MA
{33} D/C#
PR149
82.5K/F_6
{33} AC SET_EC
PC151
10U/6.3V_8X
PR153
10K/F_4
+3VPCU
PR118
10K/F_4
CSIN
CSIP
(Near by IC side)
PC107
0.1U/25V_4X
PC15 1U/10V_4X
PR20
4.7_6
PC12 1U/10V_4X
{33,35} ACIN
ACIN
PC105 0.1U/25V_4X
{33} MBDATA
{33} MBCLK
PU7
ISL88731CHRTZ-T
NC
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC
ICM
NC
GND
PR117
2.7_6
PC100
0.1U/50V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ25
AON7410
PQ22
AON7410
PL1
3.3UH_7X7
0.01_3720
PR107
PR16
*2.2/F_6
PC8
*1000P/50V_4X
PR112
10/F_6
PR113
10/F_6
PC84
10U/25V_8X
PC82
10U/25V_8X
PC13
0.1U/25V_4X
PR18
49.9/F_6
DCIN
PR130
82.5K/F_6
3.2V
88731ACIN
PR131
22K/F_6
PC101
0.1U/25V_4X
(Near by IC side)
CSOP
CSON
PR115
100_4
BAT-V
(Please place this R near by battery pack side)
PR21
2.21K/F_6
PC21
0.01U/50V_4X
PC18
*1U/10V_4X
PC17
0.01U/50V_4X
PR120
100_4
ICMNT {33}
PC110
10U/6.3V_8X
10/10/01 change Value and FP (EMI)
10/10/05 change Value and FP (EMI)
10/10/06 PC71 and PC76 預留
*0.1U/25V_4X PC95
*2200P/50V_4X PC96
10U/25V_8X PC97
10U/25V_8X PC98
*E@10U/25V_8X PC10
*E@10U/25V_8X PC11
B2A
PU11
CM1213A-04SO
ID
TEMP_MBAT_C
CH1
VN
CH2
CH4
VP
CH3
M-DATA
+3VPCU
M-CLOCK
B2A
D3B
PCN1
BTJ-09HZ0B
PR11
*100K_4
PR10
10K/F_4
PF1
F1206HA15V024TM
MBAT+
BAT-V
ID
{33}
TEMP_MBAT_C
M-DATA
M-CLOCK
PC2
47P/50V_4N
PR6
100/F_4
PC1
PR7
100/F_4
47P/50V_4N
MBDATA {33}
MBCLK {33}
PD1
*UDZSTE-175.6B
PD2
*UDZSTE-175.6B
D3B
PR8
100K_4
1K_4
PR9
TEMP_MBAT {33}
PC3
0.01U/50V_4X
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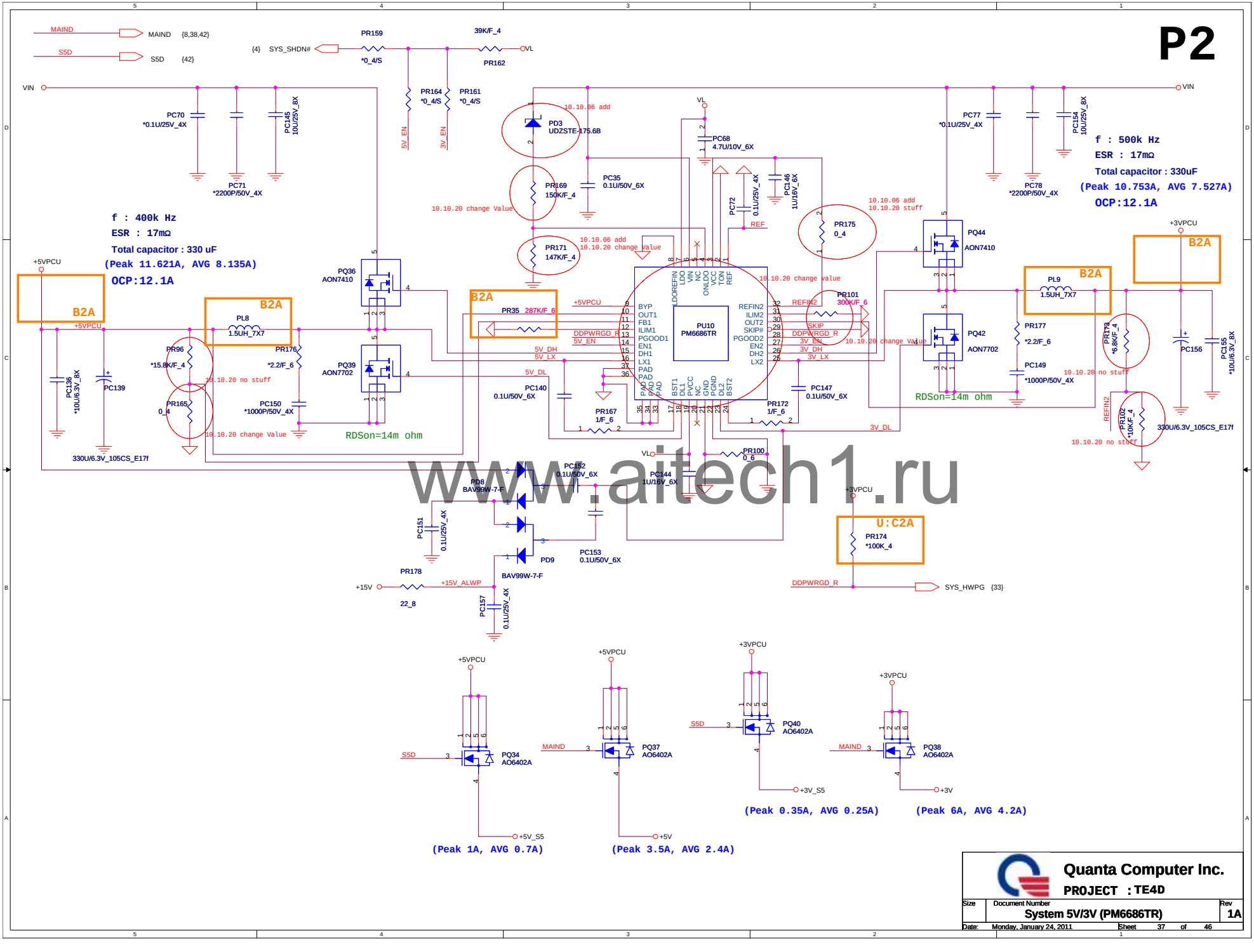
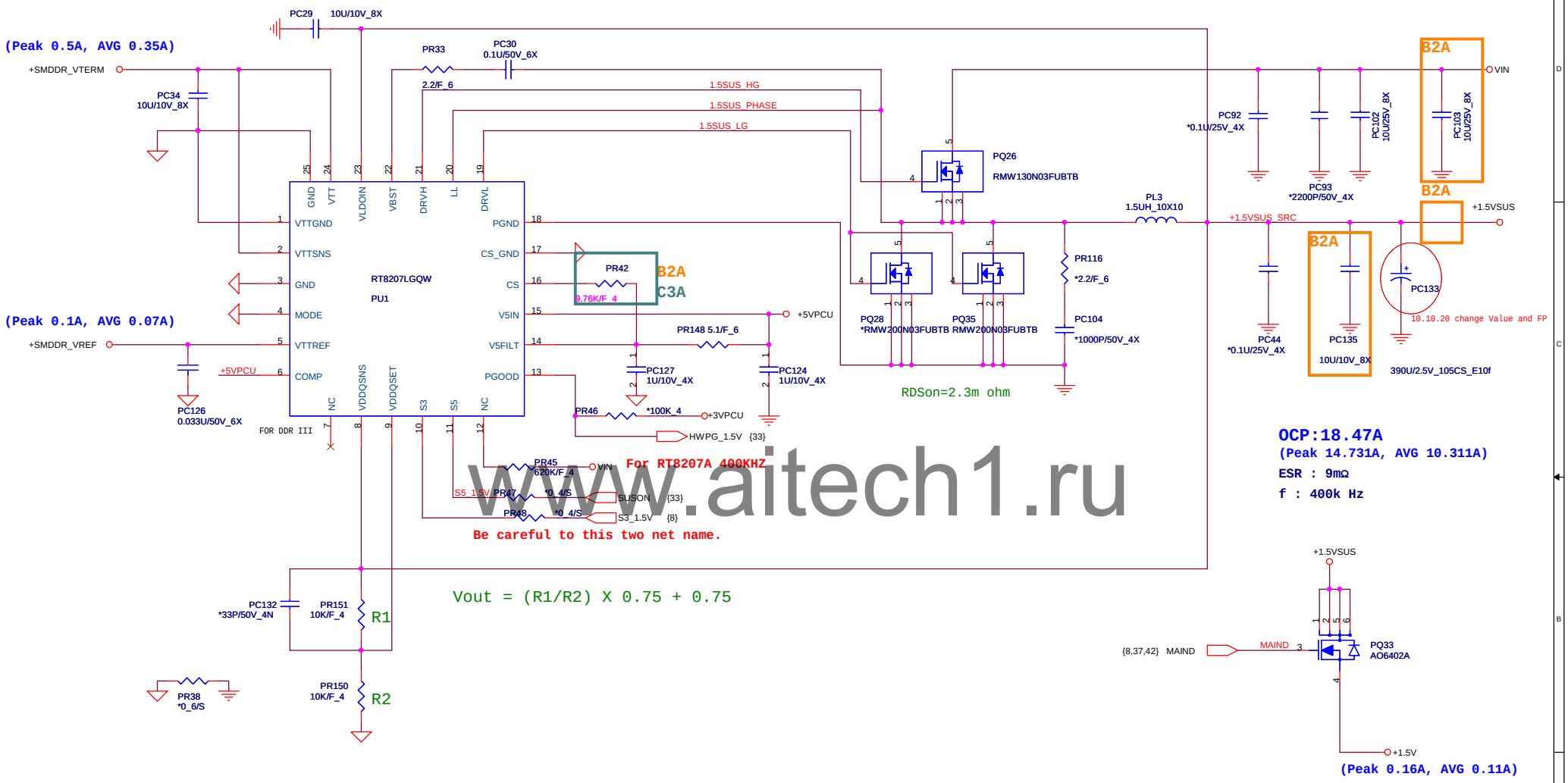
Quanta Computer Inc.
PROJECT : TE4D
Size
Document Number
CHARGER-ISL88731C
Rev
1A
Date: Monday, January 24, 2011
Sheet 36 of 46



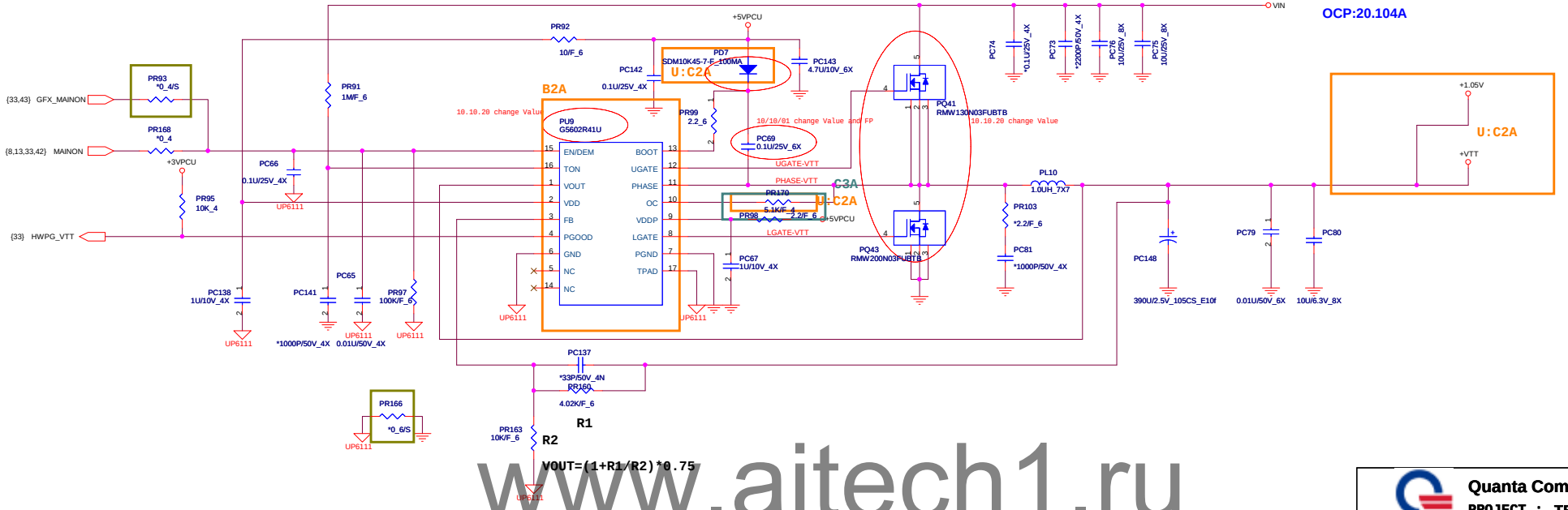
P3



Quanta Computer Inc.		
PROJECT : TE4D		
Size	Document Number: DDR 1.5V(RT8207L)/1.05VSUS	Rev 1A
Date: Monday, January 24, 2011	Sheet 38 of 46	

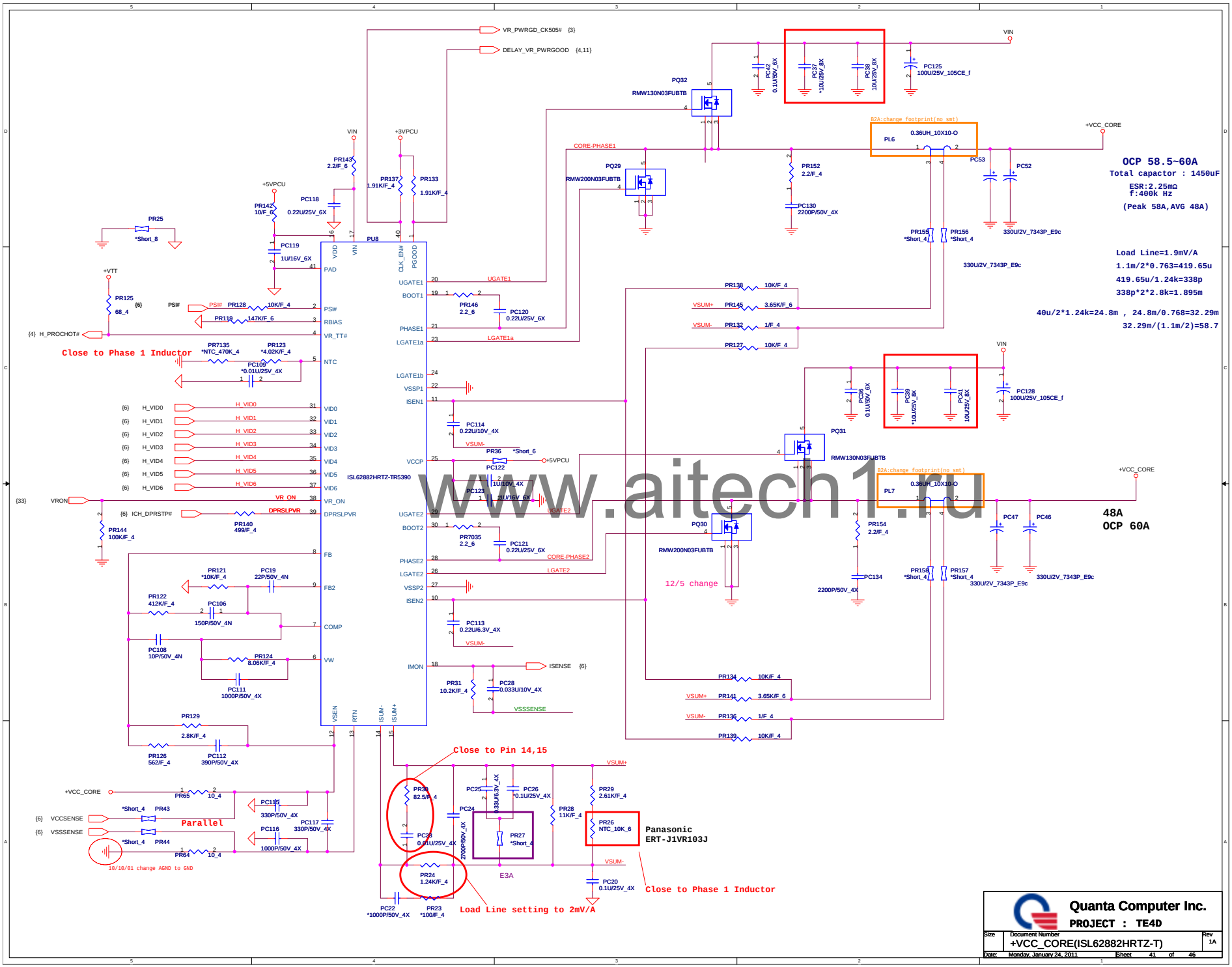
P4

Total capacitor : 390uF
F: 320k Hz
(Peak 28.220A , AVG 19.754A)
OCP:20.104A

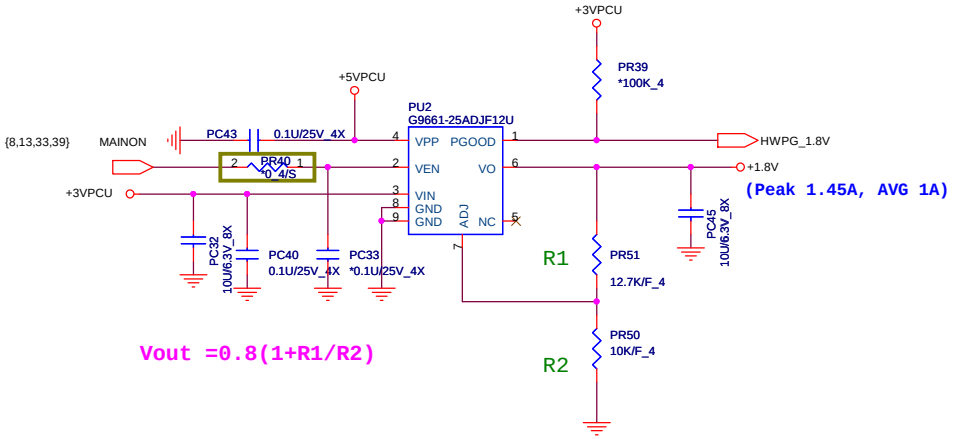


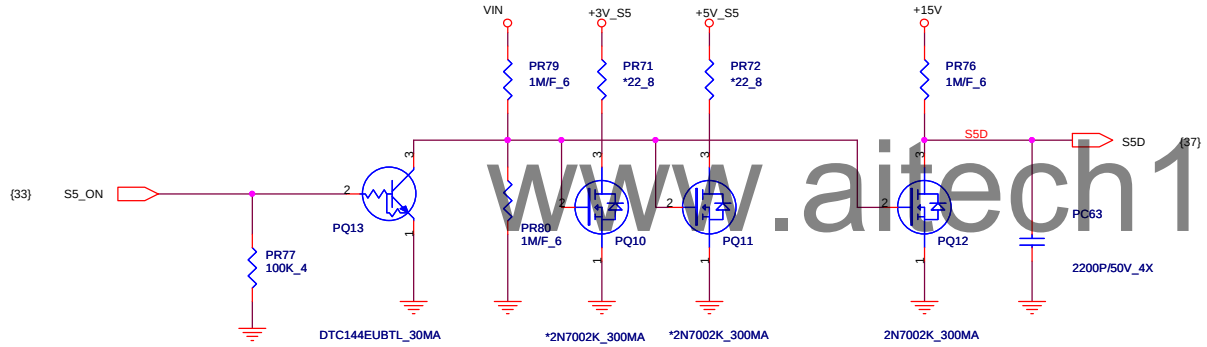
Quanta Computer Inc.
PROJECT : TE4D

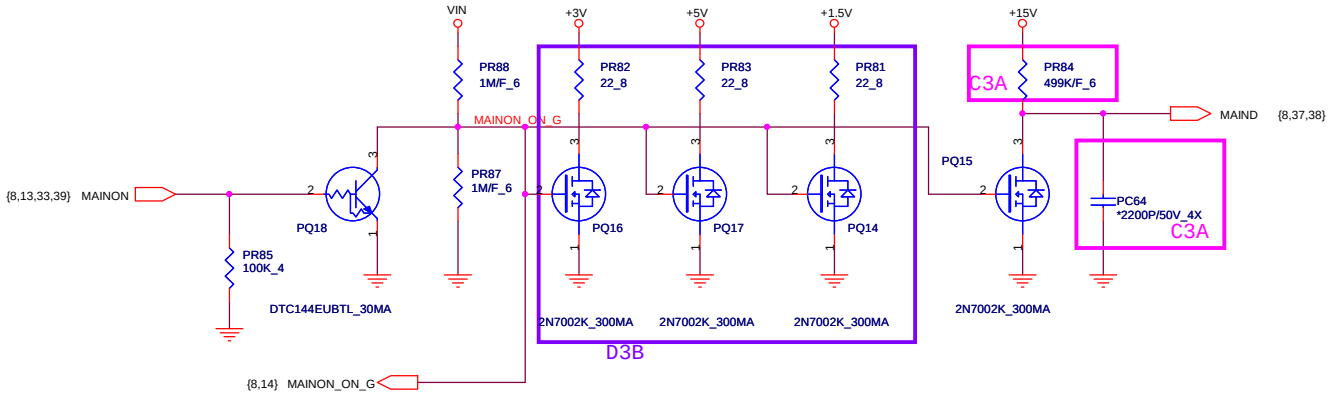
Size	Document Number	Rev
	+VTT/+1.05V (G5602R41U)	1A
Date: Monday, January 24, 2011	Sheet 39 of 46	



P7

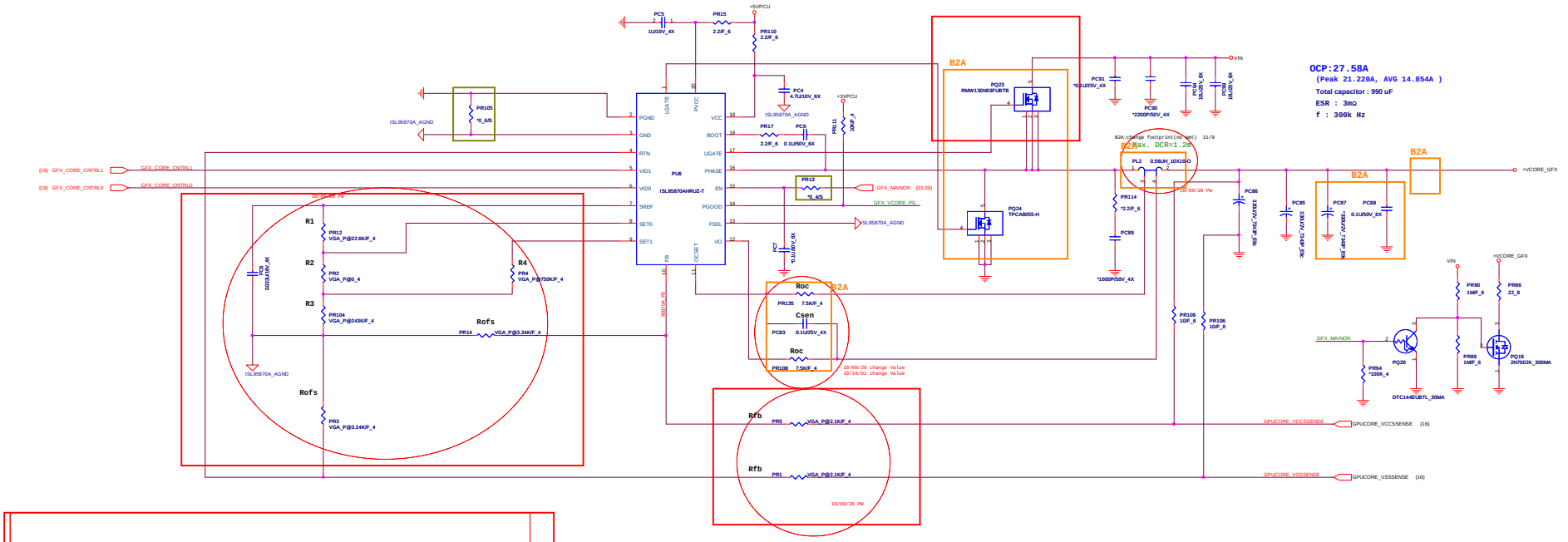






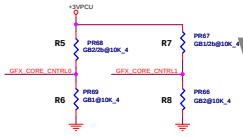
Quanta Computer Inc.		
PROJECT : TE4D		
Size	Document Number: +1.8V (G9661A)/Discharge	Rev: 1A
Date: Monday, January 24, 2011	Sheet 42 of 46	

P8 - VGA



Need to consider DOS mode

Default		N12M-GE @GB1	N12P-LP @GB2	N12P-GV
PR68	R5	NC	10K CS31002JB28	10K CS31002JB28
PR69	R6	10K CS31002JB28	NC	NC
PR67	R7	10K CS31002JB28	NC	10K CS31002JB28
PR66	R8	NC	10K CS31002JB28	NC

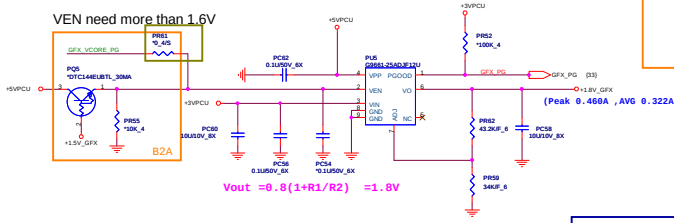


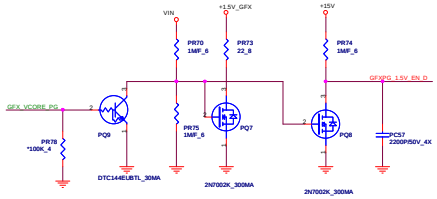
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12M-GE	N12P-LP	N12P-GV
LOW	LOW	1.0V	0.925V	1.025V
LOW	HIGH	1.0V	0.90V **Default**	1.0V
HIGH	LOW	1.0V **Default**	0.9V	1.0V
HIGH	HIGH	0.85V	0.825V	0.85V **Default**

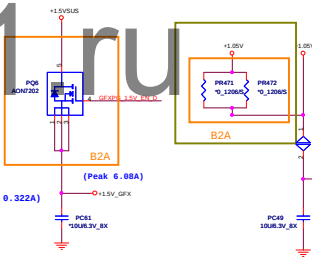
		N12M-GE @GB1	N12P-LP @GB2	N12P-GV @GB2b
R1	PR12	47.5K/F_4 CS34752FB14	22.6K/F_4 CS32262FB15	34.8K/F_4 CS33482FB22
R2	PR2	0_4 CS00002JB38	0_4 CS00002JB38	0_4 CS00002JB38
R3	PR104	270K/F_4 CS42702JB10	243K/F_4 CS42432FB02	200K/F_4 CS42002FB12
R4	PR4	1M/F_4 CS51002FB11	750K/F_4 CS47502FB14	1M/F_4 CS51002FB11
Rfb	PR1,PR5	2.32K/F_4 CS22322FB01	2.10K/F_4 CS22102FB12	2.32K/F_4 CS22322FB01
Rofs	PR3,PR14	3.3K/F_4 CS23302FB12	3.24K/F_4 CS23242FB17	3.3K/F_4 CS23302FB12

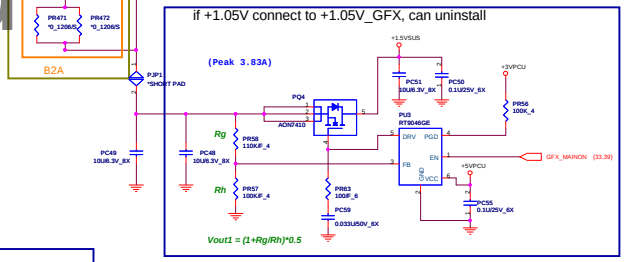
10/09/28 PM

VEN need more than 1.6V







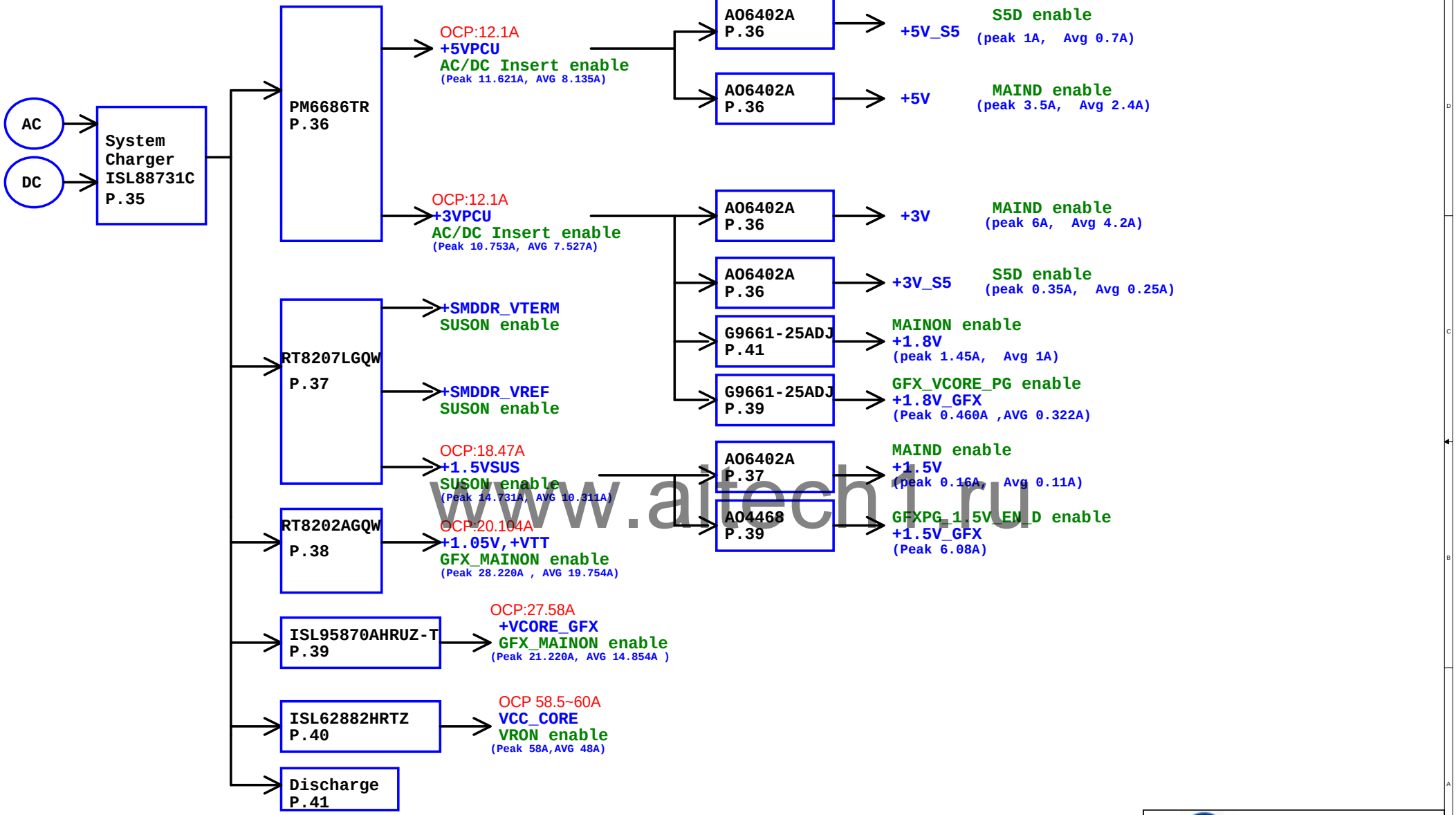


+3VPCU change to +3V
+5VPCU change to +5V

Power On Sequence
1. +3V_GFX connect +3V
2. +1.05V_GFX connect +1.05V
3. GFX_Mainon Enable +VCORE_GFX
4. GFX_VCORE_PG Enable(Delay) +1.5V_GFX
5. +1.5V_GFX Enable +1.8V_GFX
6. GFX_V18_PG connect GFX_PG

Power Off Sequence
compare +VCC3_GFX with +V1.8_GFX

Quanta Computer Inc.	
PROJECT : TE4D	
Size	Document Number: +GPU_CORE(ISL95870AHRUZ) Rev: 1A
Date: Monday, January 24, 2011	Sheet 43 of 46



Quanta Computer Inc.

PROJECT : TE4D

Size	Document Number	Rev
	POWER TREE TABLE	1A

Date: Thursday, January 20, 2011 Sheet 44 of 46

Model	REV	CHANGE LIST
TE4 MB	2A	PAGE 14: R22 no stuff PAGE 15: R23 no stuff PAGE 27: add R470 PAGE 28: add Q1100/R1015 and no stuff PAGE 32: add Q40

MODEL: TE4D

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
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24	1A	
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29	1A	
30	1A	

DOC NO. 204						
	PROJECT MODEL :	TE4	APPROVED BY:	Kent Su	DATE:	2010/11/12
	PART NUMBER:		DRAWING BY:	Kent Su	REVISON:	1A

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Model	REV	CHANGE LIST
TE4 MB	1A	PAGE 38: PC212 change value and FP to 0.1U/25V_6X ; add PD9 (10.10.06)
		PAGE 35: add PC71 and PC76 for EMI Sol. (10.10.06)
		PAGE 36: add PD12 , PR142 and PR139 (10.10.06)
		Rename
		PAGE 36: PR169 , PR171, PR165 , PU10 , PR101 change Value ; PR173 , PR102 , PR96 no stuff ; PR175 stuff (10.10.20)
		PAGE 37: PC133 change Value and FP (10.10.20)
		PAGE 38: PU9 , PQ41 , PQ43 change Value (10.10.20)

MODEL: TE2

PAGE	FROM	To
1	1A	
2	1A	
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